ISPSD 2021
SiC-P13
The 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)
May 30 – June 3, 2021, Nagoya Full Virtual Conference

Effect of gate-source bias voltage and gate-drain leakage current on the short-circuit performance of FTO-type SiC power MOSFETs

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***Abstract*— As a result of short-circuit (SC) stress tests, few commercial 1.2 kV SiC MOSFETs feature fail-to-open (FTO) behavior, that is, a permanent short-circuit between gate and source terminals, even at drain-source bias voltages as high as 600 V. Such devices are very interesting from an application point of view, since such failure mode enables implementation of *hopping-home* functionality at a nominal operational voltage and have thus been investigated in depth. This work delivers incremental and complementary understanding on the very timely and highly application-relevant topic of short-circuit withstand capability, aging and failure-mode of SiC power MOSFETs, pointing out new effects and dependence of the degradation state on the bias conditions during test.**

Keywords—SiC MOSFETs; short-circuit ruggedness; hopping-home mode; robustness.

I. INTRODUCTION

It has been recently shown that:

- damage accumulation and failure in SC-FTO-type devices intervenes only for short-circuit pulses longer than a given critical value, after which the gate-leakage current increases noticeably;
- degradation and failure are the result of the creation of cracks in the top SiO_2 as a consequence of thermo-mechanical stress and subsequent temperature-related extrusion of the top metallization [1];
- subject to ad-hoc bias conditions, functionality can be recovered, as a result of metal-paths fusing effects in the device top region [2].

Here, a new result is presented and discussed, that is, the detection of leakage current flowing directly between gate and drain to also affect the short-circuit performance and robustness of the transistors, for which it is shown that the value of gate-source bias during short circuit also plays an important role.

II. EXPERIMENTAL RESULTS

A. Leakage paths after low-voltage SC stress

As schematically illustrated in Fig. 1, a typical planar-gate SiC power MOSFET features at least 4 possible gate current leakage paths over the gate-oxide. *Path 1* is represented by the gate-oxide leak to the source N^+ implants regions. *Path 2* is a variant of *Path 1*, but terminated onto the transistor channel region, in the P-well, JFET-drift regions and possibly the body diode, too. *Path 3* is a direct leakage path through the inter-cells gate-oxide and terminating directly onto the N- drift region. Finally, *Path 4*, the one which received most attention in specialist literature, is created between the gate-polysilicon and the top-side source metallic contact and through the SiO_2 inter-layer-dielectric region (ILD). *Paths 1, 2* and *4* close onto the source terminal, either directly the metal or the channel region. *Path 3* directly onto the drain.

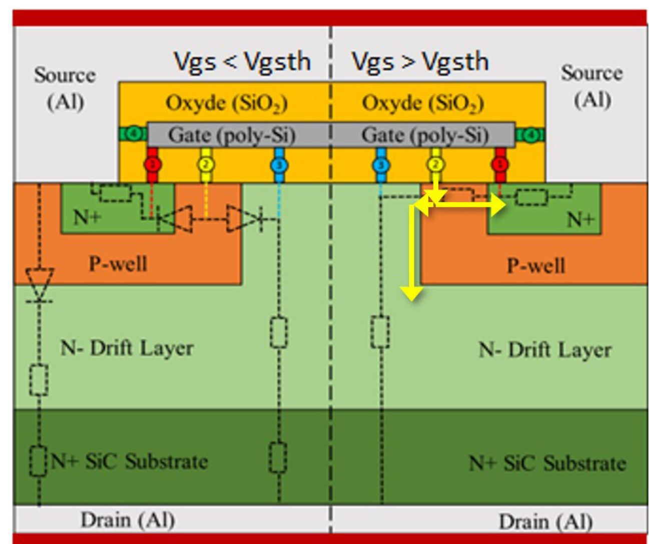

Fig. 1. Schematic depiction of SiC MOSFET cross-section with indication of 3 possible current-leakage paths between gate and source regions and 1 between gate and drain, with drain and source terminals assumed shorted with each other.

When the devices are degraded after repetitive short-circuit stress [2], the permanent gate-leakage current increases significantly and shows a pronounced dependence on the value of applied V_{GS}. Results presented here were obtained under relatively high values of the gate bias-voltage, ranging from 18V to 23V, on the same component, to amplify the electrical stress. The nominal gate-source voltage recommended by the

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manufacturer is 20 V and the maximum is 25 V in repetitive or static bias conditions. Over-biasing the gate during short-circuit with 600 V applied between drain and source leads to an excess current and power density applied to the chip ranging from 205 A for V_{GS}=18 V to 325 A for V_{GS}=23 V: an increase of 60% on the peak saturation current amplitude. However, as V_{GS} is increased from 18 V to 23 V, an additional new observation is made, which is well illustrated by the results of Fig. 2: in Fig. 2 a), a pronounced drop in V_{DS} can be observed with increasing V_{GS}; this, in turn, leads to a corresponding major drop of the gate leakage current value in the initial portion of the SC pulse, as clearly visible in Fig. 2 b).

To further clarify this observation, offline measurements were carried out on degraded devices, that is, devices which had undergone a stress sequence as per Fig. 2. The test setup and some representative test results are shown in Fig. 3: the DUTs, two SiC MOSFETs, had been previously stressed with different high V_{GS} values (21 and 23 V) and featured different degradation states, measured in terms of gate-source resistance of 529 and 770 Ω, respectively. It should be noted that these gate-resistances are 2 to 3 times lower than those measured in [1], which clearly shows the correlation between the power density applied to the chip and the impact on its accumulated gate damage, for the same stress-application time, which is between 9 µs and 10 µs. Obviously, as a result, the chip generally ages faster in repeated short-circuit cycles, a few cycles (<10) at V_{GS}=23 V, are sufficient, whereas in [1], at V_{GS}=18 V, the chip could withstand almost 1000 cycles without significant damage. As per Fig. 3, a measurement of the leakage current as a function of V_{GS} for these devices (indicated as DUT n°1 and DUT n°2)

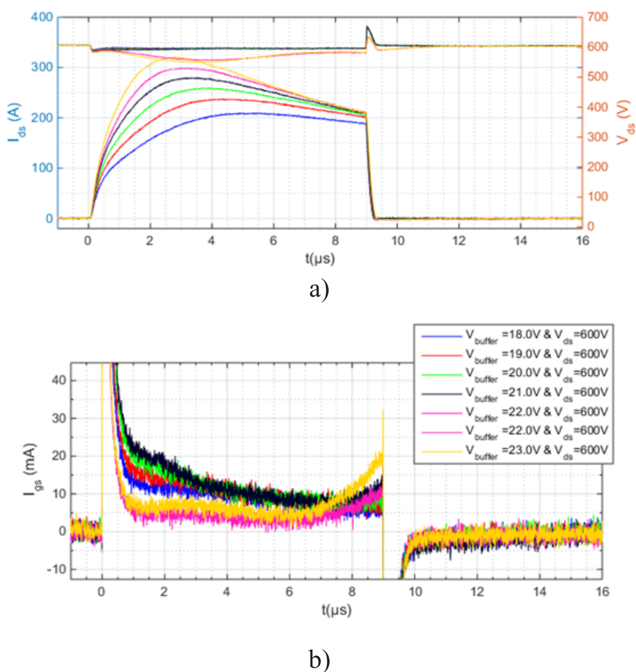

Fig. 2. (a) Short-circuit drain current (left) and drain-source voltage (right) and (b) corresponding gate leakage current for different values of gate-source bias voltage, between 18 and 23 V.

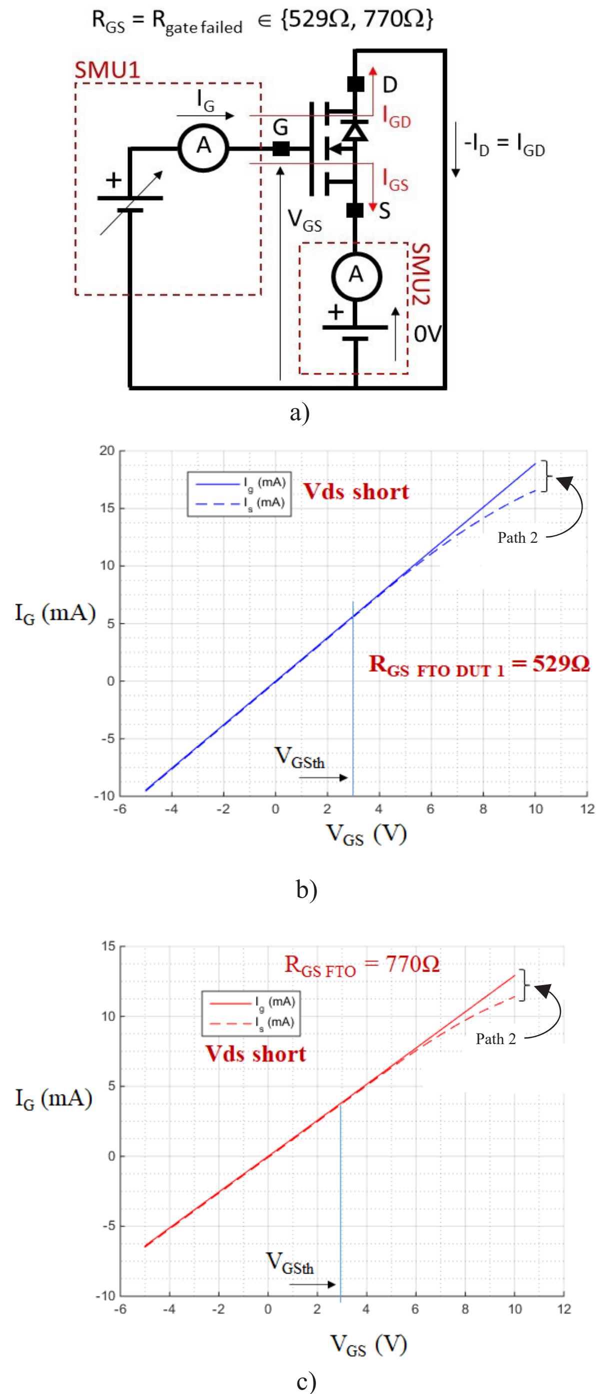

Fig. 3. (a) Schematic of experimental setup for static measurement of gate leakage and source currents for devices gate-degraded under short-circuit stress. (b) Current as a function of gate to source bias for the device stressed with SC pulses at V_{GS} = 21 V and (c) at V_{GS} = 23 V The solid line is the current measured at the gate terminal; the dashed line the current measured at the source terminal. The two curves start to diverge at higher values of V_{GS}. The drain was shorted with the source in these tests.

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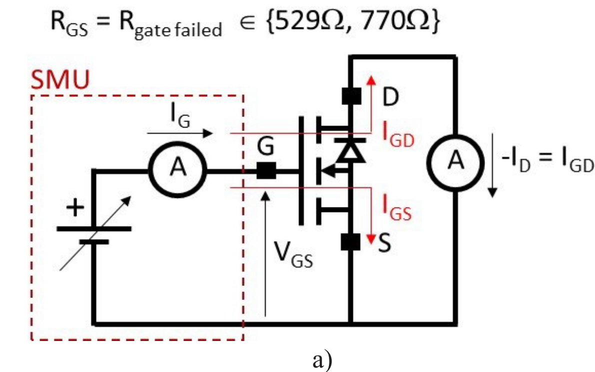
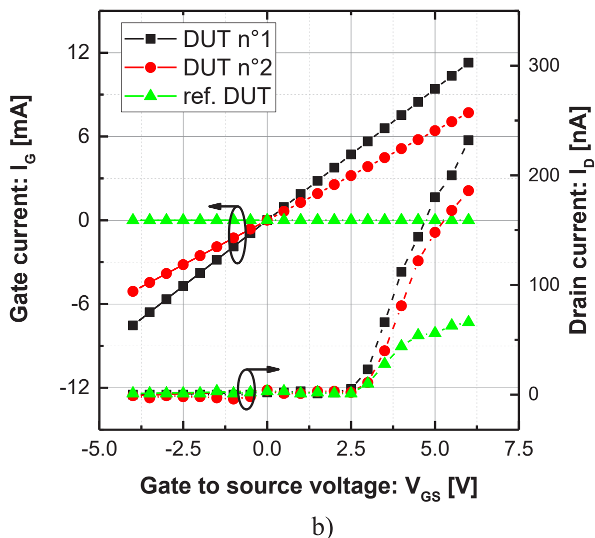
reveals, the presence of a gate current component not terminated onto the source, as highlighted by the divergence of the gate and source current values as V_{GS} is increased. Such component, which becomes significant well beyond the nominal threshold voltage value V_{TH}=3 V, is assumed to involve the channel region via *Path 2*, rather than *Paths 1* and *4*, which bypass the channel, and to be directly flowing into the drain region. The fact that such leakage component no longer appears if $V_{GS} < V_{TH}$ indicates that *Path 3* is not involved in this leakage mechanism. The measurements in Fig. 3 were carried out with a two-channel source-meter unit (Keysight™ B2902A SMU). One measured the leakage I_G through the gate and the other measured the return leakage current I_S through the source. The difference of such currents is I_G-I_S = -I_D, that is, a leakage current component over the drain. However, as the total gate leakage current is of relatively high value, I_G = 23 V/530 Ω ≅ 43 mA, it is necessary to keep a high current range on both channels. This constraint greatly reduces the accuracy of the measurement on the current difference.

To circumvent this constraint and increase the measurement accuracy, the test setup illustrated in the schematic circuit of Fig. 4 a) was used: here, the second channel of the SMU is replaced by a precision ammeter (Keysight™ 34461A) in the drain-source loop, with a measuring range adapted this time only to the measurement of the leakage current trough the drain. Measurements were carried out again on DUT n°1 and DUT n°2 and this time also compared with a measurement onto a new device of the same type (ref. DUT), serving as benchmark reference. As shown in Fig. 4 b), this new measurement confirms the first observation, that is, a significant current leakage of several hundred nano-amperes as soon as V_{GS} approaches V_{TH}, confirming the existence of a leakage through the channel and the JFET-drift region via *Path 2*. Still, no leakage is measurable if the gate voltage is negative.

In this case, if the device is left for a long time unbiased, the value of leakage current reduces significantly as compared to the value just after stress. This result thus tends to show that leakage by the ILD, as widely studied in the bibliography, is not the only path involved and that gate-oxide is also involved. In this mechanism, it should be noted that the body diode cannot conduct because it is short-circuited by the very low resistance of the drain measuring circuit, which consists of an ammeter without any threshold voltage, as it is not an SMU channel. An accurate failure analysis in the gate-oxide region is required to definitively confirm these results and analysis. That is quite



a)



b)

Fig. 4. Direct measurement of gate-drain current leakage with dedicated test setup applied on a gate-damage device.

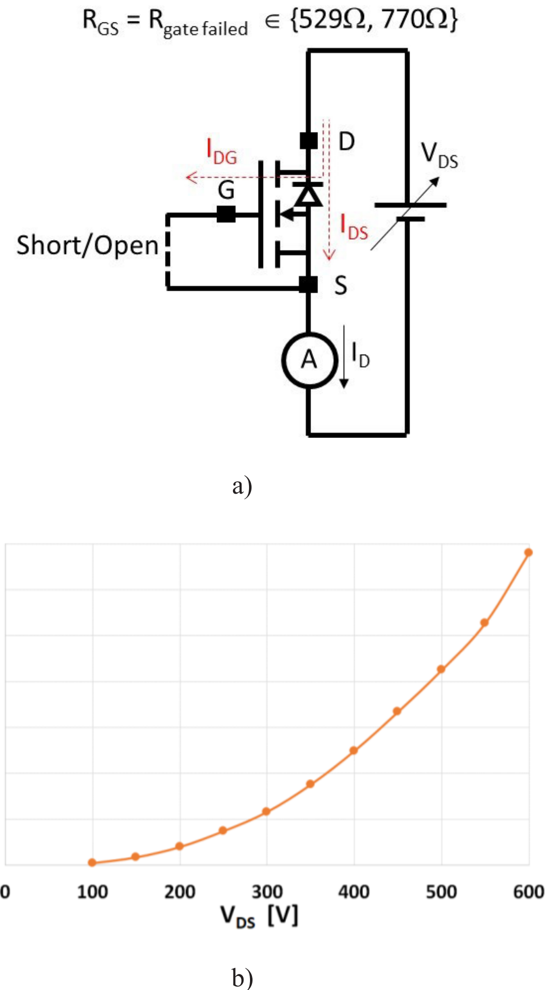


Fig. 5. Direct measurement of drain-gate current leakage with V_{GS}=0 V applied (shorted / opened gate-source gives the same results).

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complex due to the oxide being very thin and fine cracks very difficult to localize by classical methods such as lock-in thermography or Optical Beam Induced Resistance Change. The Al source metallization on top of the chip provides a shield which weakens the sensitivity of failure detection.

B. Leakage paths after high-voltage SC stress

In this work, we also explored another consequence of the gate-damage failure-mode. In Fig. 5, when the drain is biased at high voltage, but with $V_{GS} = 0$ V or V_{GS} open, the leakage current is significantly higher than the value of the new *reference* device. At $V_{DS} = 400$ V, the leakage of a damaged device is 5 nA whereas it is less than 50 pA on a new device. This leakage was also partially highlighted in [3] with a comparable value, on a different reference DUT, but with the same voltage rating and comparable active surface area, also subjected to a comparable energy stress level. However, its origin has yet to be found. Several hypotheses can be put forward:

- either a small crack in the gate oxide of the JFET intercellular region: this defect path would parallel the defect in *Path 2* discussed above;
- or a damage of the peripheral regions (i.e., field oxide and nitride at the top of the chip) of the device due to the thermo-mechanical stress applied in short-circuit operation.

However, this measurement on a damaged component is not always stable within the same measurement or reproducible from one test to another. This problem is frequently encountered when electrical characteristics are measured on a component whose damaged state is not fully stabilized, particularly when it involves metallurgical and mechanical phenomena whose relaxation and diffusion constants may be long or evolving.

C. Optical analysis of the failure mode

Finally, lock-in thermography tests on degraded devices indicate leakage not only on the running-gate finger: hot-spots on the active area are also detected, clearly visible in the results of Fig. 6 a). It is interesting to note that, in this case, too, just as highlighted in [2], the devices feature partial recovery of the accumulated damage by ad-hoc off-line biasing, Fig. 6 b).

III. Conclusion

SiC MOSFETs exhibiting a safe type of failure as a result of short circuit stress are of particular interest from an application perspective. In this paper, the degradation, and aging effects of repetitive short circuit tests on this class of devices have been investigated. Measurements conducted on devices with different grades of degradation have shown the insurgence of a drain leakage current that does not flow through the source of the device. The occurrence of such a current only for values of gate bias above the threshold voltage suggests that the damaged area of the device also involves the gate oxide above the channel region. However, an accurate failure analysis is necessary to confirm this finding and exactly locate the damaged region. Furthermore, leakage current flowing from drain to source has also been observed at high drain-to-source bias (>100 V). This might be attributed either to a crack in the gate oxide or to a damage in the termination region of the device.

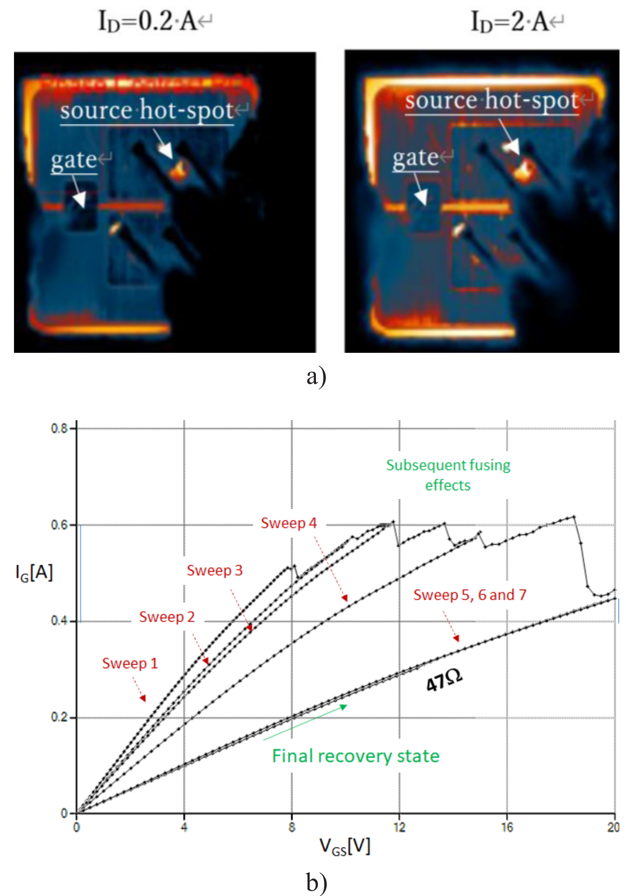

Fig. 6. Lock-in thermography on degraded chip, under different drain current values for the same V_{GS} bias (left): next to leakage in the running gate-finger, a hot-spot on the source pad is also detected. Progressive recovery effect by dedicated off-line tests (right), with the device reaching a final stable state (characterized however by excessive gate leakage current for realistic use in application).

IV. References

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