An Embedded Resolver-to-Digital Conversion Method Using Resonant Excitation and Quality-Driven Autotuning

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***Abstract*—Resolvers are widely used in safety-critical and harsh environments due to their robustness against temperature, vibration, and electromagnetic interference. Conventional resolver-to-digital converters (RDCs) often rely on monolithic integrated circuits (ICs) integrating excitation, demodulation, and tracking loops, which add cost and board footprint while limiting flexibility. This article presents a fully embedded RDC that eliminates dedicated RDC ICs by exploiting PWM and ADC resources of modern microcontrollers (MCUs). The method combines: 1) a GaN half-bridge resonant excitation engineered to align resolver sine/cosine peaks with ADC sample-and-hold instants; 2) differential 16-bit ADC acquisition with hardware PWM–ADC synchronization at sub-10-ns resolution; and 3) a software phase-locked loop (PLL) with quality-driven autotuning that minimizes the ripple of a monitoring function to optimize sampling timing and performs automatic gain/offset calibration. Experiments on a 1.1-kW PMSM test bench comparing the proposed method with a commercial RDC-IC channel show comparable or superior position/speed accuracy (ripple < 0.5%), finer velocity quantization, robust tracking during acceleration, and significant reductions in cost and PCB area. The results indicate that excitation engineering and metric-based autotuning are effective enablers for next-generation embedded resolver interfaces in electric drives.**

***Index Terms*—Autotuning, embedded systems, instrumentation for electric drives, permanent magnet synchronous motor (PMSM), phase-locked loop (PLL), position estimation, resolver-to-digital conversion (RDC), resonant excitation.**

I. Introduction

RESOLVERS are widely adopted in safety-critical and harsh-environment applications such as aerospace, railway traction, and industrial motor drives because of their robustness against temperature, vibration, and electrical noise. Functionally, a resolver can be modeled as a variable transformer whose stator windings generate sinusoidal signals proportional to the sine and cosine of the rotor angle. When properly excited and demodulated, resolvers provide absolute position information with high reliability and virtually unlimited rotational range, making them especially attractive compared to optical encoders in demanding environments [1], [2].

The conversion of resolver analog outputs into digital position and speed estimates is performed by resolver-to-digital converters (RDCs). Traditional approaches employ dedicated integrated circuits (ICs), such as AD2S1210 Analog Devices[1] [3], which incorporate excitation generation, demodulation, and a tracking loop. These ICs guarantee high accuracy and bandwidth, and are standardized in industry, but introduce several drawbacks: increased bill of materials (BOMs) cost, larger PCB footprint, and limited flexibility in tuning their internal control parameters. In addition, the dependence on monolithic solutions may hinder adaptability in applications requiring custom excitation schemes or integration into heterogeneous embedded platforms.

To address these limitations, the research community has proposed several alternative RDC implementations. Early work focused on simplified mixed analog–digital circuits aiming to reduce costs while maintaining acceptable accuracy. Attaianese et al. [4] presented a low-cost RDC using a combined analog–digital board, where the excitation of the resolver was derived from the system clock, and the position was estimated through an arctangent operation implemented with a microcontroller or EPROM-based lookup table. Although effective in reducing complexity, this approach remained constrained by the resolution of the ADC and sensitivity to analog disturbances.

In the last decade, more advanced digital approaches have been reported. Wang et al. [5] introduced a polynomial-approximation-based RDC, achieving a sub-0.002° error by combining the third-order rational fraction approximation with least-squares compensation. Zheng et al. [6] developed an FPGA-based RDC using synchronous peak sampling, coordinate rotation digital computer (CORDIC) processing, and closed-loop tracking, capable of high dynamic response and multichannel scalability. Di Tommaso et al. [7] demonstrated a simple software-based RDC algorithm in which resolver signals are processed directly by microcontrollers or FPGAs and experimentally validated against incremental encoders. These works confirm a growing trend toward flexible, processor-based RDC schemes capable of seamlessly integrating with modern motor control systems.

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In this context, this article proposes a novel embedded RDC method that eliminates the need for dedicated converter ICs by leveraging the internal resources of modern microcontrollers (MCUs). The contribution of this work is threefold.

1) *Excitation Engineering:* A multiphase resonant cycle that maximizes SNR at ADC S/H instants.
2) *Quality-Driven Autotuning:* Automatic search of excitation time constants and sampling delay that minimizes a monitoring-signal ripple; plus automatic gain/offset correction.
3) *Real-Time Integration:* Hardware-synchronized PWM–ADC triggering with ~10-ns granularity; processing in a slave task (ST) that overlaps the main control ADC activity.

Monolithic RDC IC solutions currently available to the industry (e.g., AD2S1210), integrate excitation generation, demodulation and a tracking loop, providing standardized performance and high tracking bandwidth with a compact, drop-in interface. However, their internal architecture and timing are largely fixed, which limits: 1) the possibility of shaping the excitation waveform to maximize SNR at specific sampling instants; 2) the flexibility to co-design the analog front-end (AFE) and sampling timing with the application constraints; and 3) the ability to implement application-specific autotuning and monitoring strategies beyond the IC built-in functions.

The proposed embedded RDC targets a complementary design point: it leverages PWM and differential ADC resources of MCUs to co-design excitation and acquisition. Specifically, the excitation cycle is engineered to place sine/cosine maxima at the ADC sample-and-hold instant, and a quality-driven autotuning procedure automatically refines timing and gain/offset calibration based on a measured ripple metric. This improves configurability (excitation cycle, timing, bandwidth, and calibration policies) and enables the tight integration with the drive-control firmware, at the price of careful excitation/analog co-design and the need for suitable MCU timing/ADC resources. A concise comparison is provided in Table I.

The proposed method has been experimentally validated on a 1.1-kW permanent magnet synchronous motor (PMSM) drive, where its performance was compared to a commercial AD2S1210-based RDC. The results show that the embedded approach achieves comparable accuracy in position estimation, while significantly reducing the hardware cost and footprint. Moreover, its configurability allows tailoring of the excitation waveform, bandwidth, and tuning parameters to the specific application, which is not feasible with fixed-function monolithic ICs.

The remainder of this article is organized as follows. Section II reports on related works. Section III describes the hardware architecture, including excitation generation and AFE conditioning, and details the digital processing algorithms, with an emphasis on PLL design and autotuning procedures. Section IV presents the experimental validation and comparison with a monolithic RDC under both steady-state and dynamic conditions. Eventually, Section V summarizes the conclusion.

TABLE I
QUALITATIVE COMPARISON BETWEEN MONOLITHIC RDC ICS AND THE PROPOSED EMBEDDED RDC

Aspect	Monolithic RDC IC	Proposed embedded RDC
Excitation waveform	Sinusoidal waveform with limited options	Fully programmable resonant waveform
Synchronization	External digital asynchronous S/H signal	S/H aligned with sub-10 ns resolution to engineered maxima by hardware synchronization
Tuning flexibility	Limited internal parameters	Timing, excitation, and calibration policies tunable in firmware
Calibration	Typically limited	Online gain/offset calibration + quality-driven timing autotuning
Integration	External IC interface (SPI/parallel)	Native MCU task integration
Scaling	Additional IC per channel	Additional AFE per channel; subject to ADC/PWM availability
Main advantages	Drop-in, standardized performance	Configurable excitation/acquisition co-design, autotuning, reduced IC count
Main trade-offs	Less flexible, fixed architecture	Requires careful analog/excitation co-design; depends on MCU resources

II. RELATED WORKS

Resolver-to-digital conversion (RDC) has been traditionally addressed through tracking-converter architectures, where synchronous demodulation feeds a closed-loop angle/speed tracking system. Classic discussions on resolver signal requirements, accuracy drivers, and tracking-loop behavior can be found in [1], [2], and [8]. In industrial practice, monolithic RDC ICs (e.g., AD2S1210) integrate excitation generation, demodulation and a tracking loop, providing standardized performance but limited flexibility in excitation shaping and internal parameter tuning.

To overcome IC constraints and improve integration, several all-digital and processor-based approaches have been proposed. Fully digital or mixed-signal RDCs have been reported for high-accuracy conversion and embedded drives, including all-digital architectures and DSP-based implementations with software tracking and compensation [9], [10], [11], [12], [13]. FPGA-based solutions have also been explored to combine synchronous demodulation, peak sampling, and high-bandwidth tracking loops in multichannel setups [6], [14].

Regarding excitation and demodulation strategies, beyond sinusoidal excitation, square-wave excitation has been analyzed and exploited to simplify drive and processing while retaining high conversion accuracy [15]. In parallel, open-loop computational methods based on polynomial/rational approximations and quadrant reconstruction have been proposed

for PMSM control [5]. Observer-based and hybrid schemes have also been investigated to enhance the robustness under speed variations and disturbances [16]. Moreover, calibration techniques (gain/offset and harmonic/distortion compensation) have been shown to be crucial in practical RDCs [17].

Building on this landscape, the present work specifically targets a fully embedded RDC tightly integrated with the MCU timing resources. Differently from approaches that assume a fixed excitation waveform and focus mainly on digital postprocessing, we co-design: 1) a resonant excitation cycle to place sin/cos maxima at the ADC S/H instants and 2) a quality-driven autotuning procedure that optimizes timing and corrects gain/offset within a unified embedded workflow.

III. Proposed Hardware Architecture

As is well known, with reference to a two-pole resolver with rotor excitation $v_e(t) = V_e \cos(\omega t)$ and shaft angle $\theta(t)$, the voltages of the two stator resolver windings (neglecting small speed terms when the angular excitation frequency ω is high) are

$$v_d(t) \approx k_e V_e \cos\theta \cos(\omega t) \quad (1)$$

$$v_q(t) \approx k_e V_e \sin\theta \cos(\omega t) \quad (2)$$

with k_e being the stator/rotor transformer ratio. The effect of the neglected motional terms is discussed in Appendix C. To get the rotor position θ, these voltages have to be adequately conditioned, sampled, and digitally converted. Synchronous sampling at fixed excitation phase avoids zero crossings; aligning sampling to peaks improves signal-to-noise ratio (SNR), reduces phase-locked loop (PLL) phase jitter, and maximizes ADC range usage.

A. Operating Principle

Within embedded systems used for electric drive control, the proposed method is an alternative to monolithic RDCs typically used to excite and read resolvers. By leveraging embedded resources, both the excitation driving and the acquisition of the sine/cosine voltages of the resolver are delegated to the PWM/ADC modules integrated in the embedded platform. The sine/cosine signal processing is handled by a software ST running on the embedded microcontroller unit (MCU). ST is synchronized with the software master task (MT) that executes the drive control algorithm. This implies that sine/cosine sampling must occur at the MT sampling frequency f_s. To maximize position-estimation accuracy, it is crucial to trigger the digital conversion of the sine/cosine voltages at the maximum of the resolver secondary voltage, compatible with magnetic saturation limits. In other words, a periodic resolver excitation (not necessarily sinusoidal) must be produced at the sampling frequency, and each excitation cycle must be synchronized so that the peaks of the sine/cosine signals coincide with the sample-and-hold instant of the corresponding secondary ADC channels (SACs). The driver and conditioning circuits described below are designed to meet this requirement.

At the end of the sample-and-hold window, ST processes the digitized signals and outputs the position/speed estimate. In dual-processor embedded systems, ST can run on the secondary core, so that the ST execution time is masked by the acquisition time of the main ADC channels (MACs) used by MT, provided that ST is triggered in sync with the main ADCs.

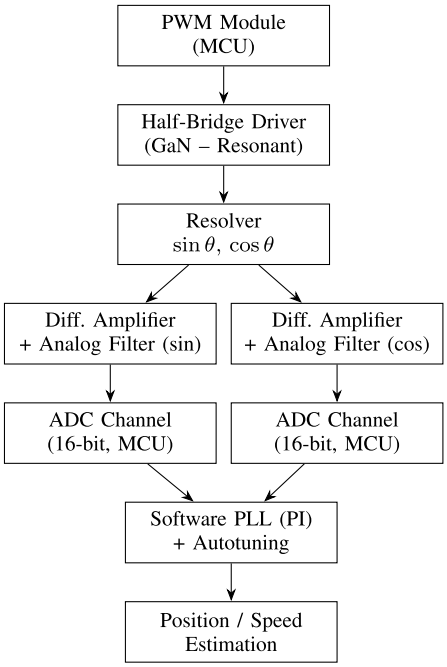

Fig. 1. Block diagram of the proposed hardware architecture.

In the current implementation, the resolver sine/cosine voltages $v_q(t)/v_d(t)$ are produced by the resonance excitation strategy (see Section III-B) while a software PLL (see Section III-E) running in the ST processes the conditioned voltages $q(t)/d(t)$, which are generated by the corresponding sine/cosine voltages through two identical low-pass filters (LPFs) with passband fractional gain G (see Section III-C). In this context, let $m = (d^2 + q^2)^{1/2}$ be defined as the RDC monitor signal. Note that if the excitation cycle and the SACs triggering are configured correctly, m does not vary with θ. The amplitude of m is related to how well the full scale of SACs is utilized; the resolution of SACs is fully exploited when m corresponds to the maximum conversion value of SACs. Therefore, m is used to monitor the quality of the acquisition of sine/cosine: a smaller ripple of m over one revolution implies higher position accuracy and a larger amplitude of m implies a finer position resolution.

Fig. 1 shows the hardware architecture of the proposed method, represented by the flow: MCU PWM → GaN half-bridge resonant driver → resolver → differential analog front-end (AFE) → dual 16-bit differential ADCs → software PLL + autotuning → angle/speed outputs. Resolver sampling is hard synchronized to PWM edges by hardware triggers; RDC runs in a ST phase-locked to the control task.

B. Resonant Excitation Strategy

The driver and conditioning circuits are shown in Fig. 2. The driver is a half-bridge built around the TI LMG5200 GaN power stage with integrated drivers, commanded by the switching functions s_H and s_L generated by one of the PWM

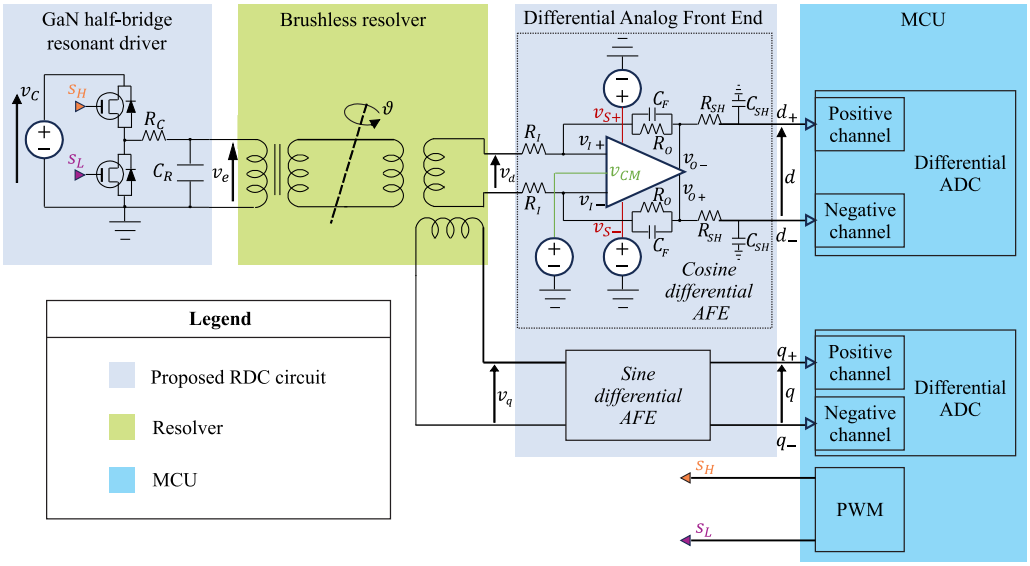

Fig. 2. Resonant driver and analog front-end.

modules available on the embedded MCU. In the prototype, $v_C = 15$ V, $R_C = 7\ \Omega$, and $C_R = 50$ nF.

The half-bridge executes a four-phase cycle per sample: 1) controlled resonant capacitor charging phase; 2) open-bridge resonance phase; 3) optional controlled discharging phase; and 4) open-bridge free evolution phase. The SACS' sampling instant is positioned in phase 2.

Specifically, the converter can operate in three modes, combined in a specific four-phase sequence for each resolver excitation cycle.

1) $\boldsymbol{s_H = 1, s_L = 0}$ *(Active Charge):* Activated at the beginning of the kth excitation cycle (instant $t = t_0^{(k)}$), and held for T_C. With $T_C > 3R_CC_R$ (i.e., $> 1\ \mu$s in the current setup), after charging the resonant capacitor to V_C, the excitation voltage v_e is kept constant for the rest of the interval. In this phase, the magnetizing current of the resolver excitation circuit increases approximately linearly.
2) $\boldsymbol{s_H = 0, s_L = 0}$ *(Induced Resonance):* after the charge time T_C, at $t = t_1^{(k)}$, with $t_1^{(k)} = t_0^{(k)} + T_C$, both half-bridge MOSFETs are turned off. A resonant exchange at angular frequency ω_R starts between the capacitor and the excitation of the resolver; the capacitor energy is transferred (losses aside) to the resolver's magnetic circuit during the phase duration T_R. The magnetizing current keeps increasing with a pseudo-sinusoidal law. It is advantageous to sample the sine/cosine windings in phase 2, setting the SAC sample-and-hold instant $t_{SH}^{(k)}$ with an appropriate delay $\Delta_{SH}^{(k)}$ from $t_1^{(k)}$, i.e., $t_{SH}^{(k)} = t_1^{(k)} + \Delta_{SH}^{(k)}$. The delay $\Delta_{SH}^{(k)}$ is chosen so that S/H occurs at the maximum of the conditioned sine/cosine signals q/d within phase 2. If phase 3 is skipped, phase 2 lasts until the resonant capacitor is fully discharged.
3) $\boldsymbol{s_H = 0, s_L = 1}$ *(Active Discharge–Optional Phase):* after acquiring sine/cosine, the resonant capacitor is actively discharged by shortening the output for approximately $T_D = 3R_CC_R$. This prevents further increase of magnetizing current (as discussed in Appendix A), dissipating the remaining capacitor energy on the charge/discharge resistor.
4) $\boldsymbol{s_H = 0, s_L = 0}$ *(Free Evolution):* after discharging the resonant capacitor, both MOSFETs are opened again. If phase 3 is not used, phase 4 coincides with the continuation of phase 2. Regardless of phase 3 activation, at the start of phase 4 the capacitor voltage is 0 and the magnetizing current is positive. Let $I_{e,R}$ be the initial condition of i_e. Two substages occur: first (*exponential decay*), i_e charges the resonant capacitor negatively; the lower diode of the half-bridge conducts, clamping the capacitor voltage near its threshold voltage V_{th}, and the magnetizing current decays exponentially toward the negative asymptote $I_{e,F} = -V_{th}/R_i$, with R_i the resolver's input resistance. Then (*residual resonance*), as the current turns negative after the substage duration $T_F = R_iL_m \log\left[1 + (I_{e,R}/I_{e,F})\right]$, a new resonance with the input capacitor is excited, with the converter excluded.

To have sine/cosine samples ready when ST starts (ST is released at the MT sampling instants) and minimize the delay between the SACs and MACs acquisitions, it suffices to set $t_{SH}^{(k)} = t_s^k - T_{conv}$, where t_s^k is the MT sampling instant and T_{conv} is the conversion time of SACs. The placement of $t_{SH}^{(k)}$, $t_0^{(k)}$, and $t_1^{(k)}$ is completely implemented in hardware by properly configuring the ADC/PWM modules of the MCU; the placement resolution for most MCUs is typically under 20 ns. For clarity, Fig. 3 aligns the four-phase excitation strategy with the main waveforms the excitation voltage v_e, the cosine voltage v_d scaled by the corresponding LPF passband gain G, the conditioned cosine signal d and the magnetizing current i_e with the rotor at $\theta = 0°$ and $f_s = 10$ kHz. For the sake of clarity, the sampling window size of the ADCs has been assumed to be null.

As for the rationale for using the multiphase resonant excitation cycle instead of a more direct sinusoidal excitation, the following aspects jointly motivate the choice adopted for the proposed embedded RDC.

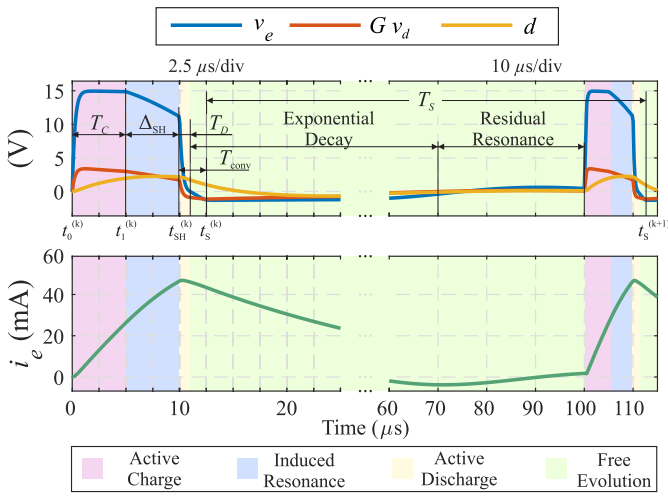

Fig. 3. Time diagram of the four-phase resonant excitation cycle.

1) Resonant excitation is naturally generated by simple half-bridge switching states (charge/open/discharge/open); conversely, the sinusoidal excitation would require, along an output power amplifier, an additional analog reconstruction filter driven by an MCU PWM (i.e., a PWM-DAC), since MCU DACs are not able to effectively synthesize low-distortion sinusoids at the required frequencies.
2) Resonant excitation admits an explicit energy-per-cycle view and therefore clear constraints on: a) rms/thermal losses; b) time/kinematic limits of the excitation cycle; and c) peak-current/saturation limits, as detailed in Appendix B; conversely, under sinusoidal excitation, thermal losses and saturation conditions depend on the frequency and amplitude of the excitation voltage through all the resolver parameters, making the operative limits more difficult to formalize.
3) Resonant excitation allows to change the sampling rate (i.e., the frequency of the excitation cycle) by just reconfiguring the timing parameters, given that the kinematic limits are respected; conversely, sinusoidal excitation requires the excitation frequency to be a multiple of the sampling frequency if peak alignment must be preserved, so that values of the sampling frequency significantly higher than the resolver rated frequency become unfeasible.

Finally, it is important to point out that high-speed operating conditions and temperature variations can cause either a real or apparent peak shifting, thus reducing the SNR achieved through the tuning of the parameter $\Delta_{SH}^{(k)}$ or introducing position estimation errors. These aspects are discussed in Appendixes C and D.

C. Analog Conditioning

The conditioning stage uses two differential amplifiers with a reference input that defines the output common mode. Fig. 2 shows the AFE used to interface the resolver cosine winding (d-quantities) to the corresponding MCU differential ADC. The AFE configuration for the sine winding (q-quantities) is identical. The scheme highlights the fully differential topology and its symmetric input/feedback network. This configuration improves the common-mode rejection ratio (CMRR) since the signals are kept differential from inputs to outputs. In the experimental prototype, the conditioning circuit is implemented by the fully differential amplifier Texas Instruments THS4151 (CMRR = –83 dB), configured to provide differential gain $G = 0.47$ (set by R_O/R_I), a controlled output common-mode $v_{CM} = 1.5$ V, and a bandwidth of approximately 100 kHz (set by $R_O C_F$), while driving the differential ADC inputs of the MCU through two decoupling filters $R_{SH} - C_{SH}$ per channel. This configuration allows to drive correctly the differential 16-bit ADC channels of most MCUs, which expect differential swings up to ±3 V, while requiring a common-mode voltage stabilized at 1.5 V.

From Fig. 2, the following input/output relationships for the cosine winding yield

$$\begin{cases} d(s) = d_+(s) - d_-(s) \\ \qquad = \dfrac{R_O}{R_I(1+sR_OC_F)(1+sR_{SH}C_{SH})} v_d(s) \\ \dfrac{d_+(s)+d_-(s)}{2} = v_{CM}(s). \end{cases} \tag{3}$$

The same applies to the outputs associated with the sine winding. Equation (3) explicitly states that the AFE enforces the output common-mode, i.e., $(d^+ + d^-)/2 = v_{CM}$, while applying the differential transfer to the input winding voltage v_d.

Design guidelines for the conditioning network include the following.

1) According to Fig. 2, $2R_I$ is the actual impedance seen by the resolver signal windings. Due to the steep excitation edge at the start of phase 1 of the excitation cycle, HF ringing, caused by resolver parasitic capacitances, can appear on the outputs and harm position estimation. A resistive load can be useful to add damping, but too low a resistance would cause excessive drops on the resolver windings. In practice, a good compromise is to choose a load significantly higher than the resolver's output impedance. In the prototype, R_I has been set to 5 $k\Omega$.
2) Once R_I has been determined as described above, the resistance R_O fixes the steady-state gain $G = R_O/R_I$ of the conditioning so that the differential outputs voltages
$$d = d_+ - d_- \qquad q = q_+ - q_- \tag{4}$$
fit the ADC's range. In the prototype, the gain is set equal to 0.47, so that a span of about ±6.4 V at the amplifier's inputs corresponds to a span of ±3 V at the ADC's inputs;
3) as required by the ADCs, the common mode is set to 1.5 V, so each single-ended node spans 0–3 V relative to the signal ground.
4) The RC filter (R_O, C_F) provides filtering to reject differential noise from the power stage and residual ringing of the magnetic circuit; this filtering significantly influences the optimal excitation-cycle configuration, as discussed in Section III-D. The bandwidth has been set equal to ≈ 100 kHz.

5) A small RC filter (R_{SH}, C_{SH}) between the amplifier outputs and the ADC inputs allows decoupling the driver from the ADC sample-and-hold; its bandwidth can typically be set ≈ 100 MHz, so its transfer function can be neglected for our purposes.

D. Simulated and Experimental Behavior of the Excitation Cycle

The excitation circuit of a brushless resolver consists of a 1:1 rotary transformer (primary on the stator, excited by v_e; secondary on the rotor), whose secondary feeds the rotor excitation circuit magnetically coupled to the two quadrature stator windings. Since the quadrature windings feed high-impedance loads, the equivalent circuit becomes a cascade of two transformers, the latter of which operates with an open secondary. Denoting by R_r the resistance of the primary winding of the rotary transformer, with R_{re} the series resistance of the secondary winding of the rotary transformer and of the excitation circuit, and with L_r and L_e being the corresponding magnetizing inductances, it can be verified that, with reference to angular frequencies ω for which $R_{re}^2/[\omega^2(L_r + L_e)L_e] \ll 1$, the input impedance Z_i of the cascaded transformers can be approximated as follows:

$$Z_i = R_r + \frac{L_r^2 R_{re}}{(L_r + L_e)^2} + j\omega \frac{L_r L_e}{L_r + L_e} \tag{5}$$

i.e., since $\Re\{Z_i\}$ is independent of the angular frequency of the resolver excitation ω, while $\Im\{Z_i\}$ varies linearly with ω, it is possible to replace cascaded transformers with an equivalent transformer for which the primary winding resistance is $R_i = \Re\{Z_i\}$ and the magnetizing inductance is $L_m = \Im\{Z_i\}/\omega$. The approximation held generally at steady state for sufficiently high excitation frequencies regardless of the excitation voltage's waveform. Consequently, an accurate response of a particular resolver to the described excitation cycle can be obtained analytically or numerically based just on the value of the resolver input impedance, which is always available in the corresponding datasheet. Moreover, the resonant capacitor can be simply sized as follows:

$$C_R = \frac{\omega_N}{\Im\{Z_i\}\,\omega_R^2} \tag{6}$$

with ω_N being the nominal angular frequency of the resolver.

1) Simulation Results: With these premises, a preliminary simulation was carried out in the MATLAB Simulink environment with reference to the two-poles 7 V–10 kHz resolver TE Connectivity V23401-S1001-B101, the model deployed in the experimental setup (see Section IV). For this resolver, as per the technical data supplied by the manufacturer, it results $R_i = 82\,\Omega$ and $L_m = 2.5$ mH, so that, given the value $C_R = 50$ nF set for the resonant capacitor on the prototype, the resulting resonant frequency is around 14.2 kHz. Fig. 4 shows the voltages v_e, Gv_d, d, and the current i_e in correspondence of one excitation cycle with the rotor at $\theta = 0°$ and $T_C = 4\,\mu$s. From the inspection of Fig. 4 one can clearly distinguish phases 1, 2, and 4 (phase 3 not used).

The maximum of d occurs in phase 2 with a substantial delay from the end of phase 1. The delay is introduced by the first-order filter with time constant $T_F = R_O C_F$ implemented in the output stages of the differential amplifiers. By assuming, for simplicity, that the exponential component of the filter output completely decays in $3T_F$, two cases can be considered as follows.

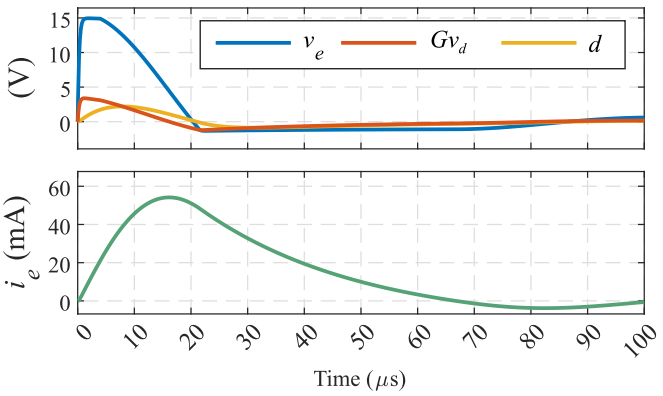

Fig. 4. Simulation of an excitation cycle.

1) $3T_F < T_C$: In this case, the filter outputs reach the inputs (which are constant in phase 1 if the resistance voltage drop driven by the magnetizing current is neglected) before the start of phase 2. Since at the beginning of phase 2 the inputs have a negative time derivative, the maximum of the filter outputs occurs in phase 1 with a delay $3T_F$ from the start of the cycle. For properly configured excitation cycles, this case never applies.
2) $3T_F > T_C$: In this case, the filter outputs are lower than the inputs at the start of phase 2. At the beginning of phase 2, the filter inputs decrease, while the filter outputs increase. The maximum occurs at the instant at which the outputs equal the inputs. To a higher T_C corresponds a lower difference between inputs and outputs and a higher time derivative of the inputs at the start of phase 2. Consequently, as T_C increases, the time delay from the start of phase 2 at which the filter outputs are maximum decreases, i.e., the maximum occurrence's time delay measured from the start of phase 1 is expected to not vary significantly with T_C.

The magnetizing current also peaks in phase 2; for the considered resolver, the nominal magnetizing peak is about 60 mA, so the cycle brings the resolver close to saturation. The peak can be reduced by driving the energy transferred to the resolver over one excitation cycle to lower values. Consequently, the peak reduction can be effectively achieved by the following.

1) Reducing T_C.
2) Reducing C_R.
3) Activating the *active discharge* phase.

Naturally, the peak reduction would also lead to a shorter duration of the *exponential decay* substage, allowing for higher frequencies of the excitation cycle. A detailed analysis of these aspects is given in Appendix A–B.

2) Experimental Results: Fig. 5 shows the oscilloscope acquisitions of v_e, d, and q over four excitation cycles at 10 kHz with the rotor at 135° and $T_C = 4\,\mu$s. The traces match the simulations (taking into account the different rotor angles). In fact, with regard to the monitor signal m, in the simulation

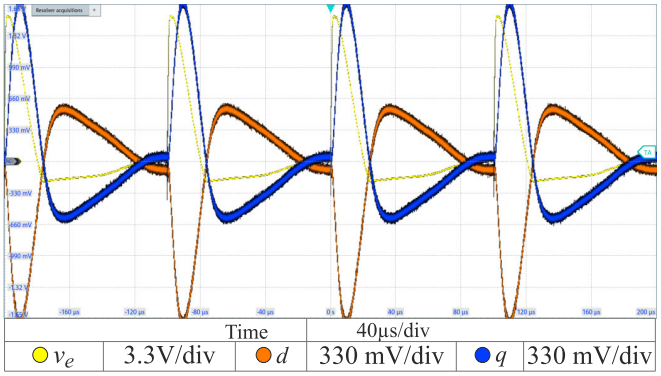

Fig. 5. Experimental excitation cycles for rotor at 135°.

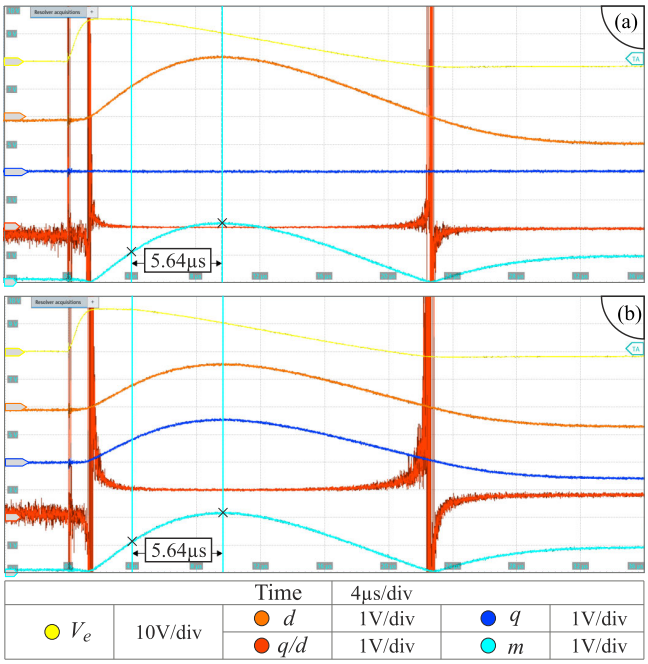

Fig. 6. Experimental excitation cycles for rotor at (a) 0° and (b) 45°.

case, it is $\max(m) = \max(d) = 2.23\ V$; in the experimental case, it is $\max(m) = \sqrt{2}\max(d) = \sqrt{2}\ 1.65 = 2.33\ V$.

Fig. 6(a) and (b) shows v_e, d, q, q/d, and m, at rotor angles 0° and 45°, respectively. The ratio $q/d = \tan(\theta)$ identifies the useful time window for placing the S/H instant, whereas m pinpoints the exact S/H placement at $\max(m)$. In both cases, the monitor amplitude is 2.21 V, and the optimal delay is $\Delta_{SH} = 5.64\ \mu s$; the invariance of $\max(m)$ and Δ_{SH} with the position of the rotor confirms the soundness of the method.

Eventually, Table II lists $max(m)$, Δ_{SH} and $T_C + \Delta_{SH}$ versus T_C: both $\max(m)$ and $T_C + \Delta_{SH}$ vary moderately with T_C, i.e., at the MT sampling instant t_s^k, the optimal activation instant of the excitation cycle $t_0^{(k)} = t_s^k - T_C - \Delta_{SH}^{(k)} - T_{conv}$ depends weakly on T_C.

E. Digital PLL Implementation and Autotuning

A type-II digital PLL with PI regulation estimates angle and speed. Let $d(k)$ and $q(k)$ be the conditioned samples acquired at the sample-and-hold instant $t_{SH}^{(k)}$. The PLL processes the signals

TABLE II
VARIATIONS OF MAIN PARAMETERS OF THE EXCITATION CYCLE VERSUS T_C

T_C (μs)	$\max(m)$ (V)	Δ_{SH} (μs)	$T_C + \Delta_{SH}$ (μs)
2.0	2.08	7.24	9.24
2.5	2.12	6.84	9.34
3.0	2.15	6.44	9.44
3.5	2.18	6.04	9.54
4.0	2.21	5.64	9.64
4.5	2.24	5.24	9.74
5.0	2.27	4.84	9.84
5.5	2.30	4.44	9.94
6.0	2.33	4.04	10.04

TABLE III
DIGITAL PLL PARAMETERS USED IN THE EXPERIMENTAL VALIDATION

Parameter	Value
Sampling period/Excitation cycle period	100 μs
Target PLL bandwidth	250 Hz
Target overshoot over step speed variation	8%
Configured proportional gain	$1.57 \times 10^3\ s^{-1}$
Configured integral gain	$61.7 \times 10^3\ s^{-2}$

$d_a(k)$ and $q_a(k)$ obtained by $d(k)$ and $q(k)$ through a preliminary offset/gain adaptation process, as detailed later in this section. The corresponding monitor signal is

$$m(k) = \sqrt{d_a^2(k) + q_a^2(k)}. \tag{7}$$

The phase detector computes a normalized phase error

$$\varepsilon(k) = \frac{-d_a(k)\sin\hat{\theta}(k) + q_a(k)\cos\hat{\theta}(k)}{m(k)} \tag{8}$$

with $\hat{\theta}(k)$ being the estimated angle. $\varepsilon(k)$ is processed by a discrete PI, whose output is the estimated resolver speed $\hat{\omega}_m$

$$\hat{\omega}_m(k) = \omega_{m,I}(k) + K_P\,\varepsilon(k) \tag{9}$$

with

$$\omega_{m,I}(k) = \omega_{m,I}(k-1) + K_I\,\varepsilon(k)\,T_s \tag{10}$$

the integral PI component. $T_s = 1/f_s$ is the sampling period (one estimate per excitation/acquisition cycle). The estimated angle is then updated as follows:

$$\hat{\theta}(k+1) = \mathrm{wrap}_{2\pi}\left(\hat{\theta}(k) + T_s\,\hat{\omega}_m(k)\right) \tag{11}$$

where $\mathrm{wrap}_{2\pi}(\cdot)$ confines the estimate to $[0, 2\pi)$ to prevent the representation overflow. The main parameters used for the experimental implementation are reported in Table III.

Two autotuning procedures are provided: 1) ADCs gain/offset autotuning procedure and 2) resonant excitation timings autotuning procedure. Both procedures process the signals' extrema observed by the extrema extraction routine (EER) over one resolver revolution. The first activation of EER is triggered after the PLL has stabilized (i.e., the estimation error stays within a steady-state identification threshold for a preset time). In each execution cycle, the procedure continuously updates the maxima and minima of (d_a, q_a, m), until one revolution is detected. This event triggers the cycle end together with the update of the observed maxima (d_M, q_M, and

m_M) and minima (d_m, q_m, and m_m) since the cycle start. If the estimation error overcomes the steady-state identification threshold at any given time, EER is reset, and its next activation is triggered, again, by PLL stabilization.

In each sampling instant, the ADCs gain/offset autotuning procedure performs input conditioning based on

$$\begin{cases} d_a(k) = d(k) - d_O(k) \\ q_a(k) = q_G(k)\ \ (q(k) - q_O(k)) \end{cases} \tag{12}$$

where the static gain q_G and offsets (d_O and q_O) are initialized, respectively, to 1 and 0 and updated upon the completion of a generic EER execution cycle as per the following:

$$\begin{cases} d_O(k) = d_O(k-1) + [d_m(k) + d_M(k)]/2 \\ q_O(k) = q_O(k-1) + \left[q_m(k) + q_M(k)\right]/2 \\ q_G(k) = q_G(k-1)\dfrac{d_M(k) - d_m(k)}{q_M(k) - q_m(k)}. \end{cases} \tag{13}$$

After the gain/offset autotuning procedure, an optional resonant excitation timings autotuning procedure determines the optimal pair (T_C, Δ_{SH}). It runs for N processing cycles, N set by the number of (T_C, Δ_{SH}) combinations to test defined by the ranges $[T_{C,m}, T_{C,M}], [\Delta_{SH,m}, \Delta_{SH,M}]$ and the corresponding steps; one can also fix T_C and sweep Δ_{SH} around an analytical/numerical guess. At each cycle start (which is synchronized to the completion of a generic EER execution cycle), the current (T_C, Δ_{SH}) are applied. The procedure then waits for two EER execution cycles to obtain reliable observed extrema, since an additional cycle is needed to optimize the ADCs gain/offsets with respect to the changed excitation timings. Upon completion of the second EER execution cycle, the monitor ripple is computed as follows:

$$m_r(k) = \frac{m_M(k) - m_m(k)}{[d_M(k) - d_m(k)] + \left[q_M(k) - q_m(k)\right]}. \tag{14}$$

After N cycles, the pair (T_C, Δ_{SH}) with minimum ripple is activated. This routine has been conceived to run once, i.e., just upon the first system activation. It can be executed while the drive is closed-loop controlled, provided that the search ranges are reasonably chosen.

Because both autotuning procedures process the extrema observed over one resolver revolution, they are more sensitive to the measurement noise than average-based statistics, since noise perturbs maxima/minima. To improve the robustness at negligible cost, the extrema extraction by EER can be based on the filtered out versions (d_f, q_f) of (d_a, q_a) by a moving-average filter of length L

$$d_f(k) = \frac{1}{L}\sum_{i=0}^{L-1} d_a(k-i), \quad q_f(k) = \frac{1}{L}\sum_{i=0}^{L-1} q_a(k-i). \tag{15}$$

Given that the filter cutoff frequency f_c is given by $f_s/(2L)$, L can be set so that f_c is one decade above the maximum expected frequency f_M of (d, q)

$$L = \text{ceil}\left(\frac{f_s}{20 f_M}\right). \tag{16}$$

It should be noted that a moving-average filter is very effective at attenuating the measurement noise (which appears in the converted signals as a superimposed oscillation at half the sampling frequency). Consequently, a low value of L is able to achieve a significant noise cancellation. For the implemented prototype, f_s = 10 kHz and f_M = 100 Hz, so that, from (16), the resultant filter window length is L = 5.

A block diagram of the whole conceived software processing approach is given in Fig. 7.

IV. Experimental Setup and Results

To perform a correct experimental comparison between the proposed method and a monolithic RDC, a testbench (see Fig. 8) has been set up using a 1.1-kW PMSM (3 pole pairs, 3000-r/min rated speed, 6000-r/min maximum speed) which has been equipped with two resolvers TE Connectivity V23401-S1001-B101 (7 V_{rms}, 10 kHz, 1 pole pair, and 0.33° maximum angular error). The motor is fed by a three-phase inverter with a 500-V DC link and coupled with the hysteresis brake Magtrol HD-805-8NA-0200. Unless otherwise specified, the tests have been performed by controlling the motor in torque mode and the brake in speed mode. Resolver 1 is excited/read by Analog Devices AD2S1210 (configured in 16-bit mode); resolver 2 uses the proposed embedded method. To provide absolute accuracy metrics, the optical encoder Heidenhain ROD 420.000B-1000 (0.09° angular resolution) has been coupled with the shaft extension of the PMSM and used as ground truth. A Texas Instruments C2000 Delfino F28379D dual-core processor operating at 200 MHz has been used as the system MCU.

A. Software Implementation

A field-oriented control (FOC) has been implemented on the MT programmed on CPU1. The task is triggered by the last end of conversion (EOC) signals generated by the configured MACs, deployed for the motor currents and the DC-Link voltage measurements. The MAC's start of conversion (SOC) signal is generated by one of the available PWM modules, selected as the reference time generator (RTG). The MCU reads the AD2S1210 position/speed through the serial peripheral interface (SPI) and the encoder position through the integrated quadrature encoder pulse (QEP) module. SACs S/H instants for the embedded RDC and position latching instants for the encoder are hardware-scheduled through proper configuration of the RTG so that they lead the S/H instants of the MACs by the SACs total conversion time. The sampling instants for the Analog Devices IC are scheduled by an ISR programmed on the CPU1 which drives low the sample pin of AD2S1210 and is triggered by one of the available CPU timers, configured to compensate for the context-switching overhead. The maximum scheduling jitter with respect to the S/H instants of the embedded RDC has been found to be around 20 ns. The phase detector routine, together with the autotuning procedures, has been implemented on the ST programmed on CPU2. The task is triggered by the RTG so that its activation is aligned with the MAC's S/H instants. Unless otherwise specified, the FOC uses position and speed supplied by the software PLL driven by the embedded RDC. Synchronization between CPUs is performed on an atomic level by exploiting the interprocessor communication (IPC)

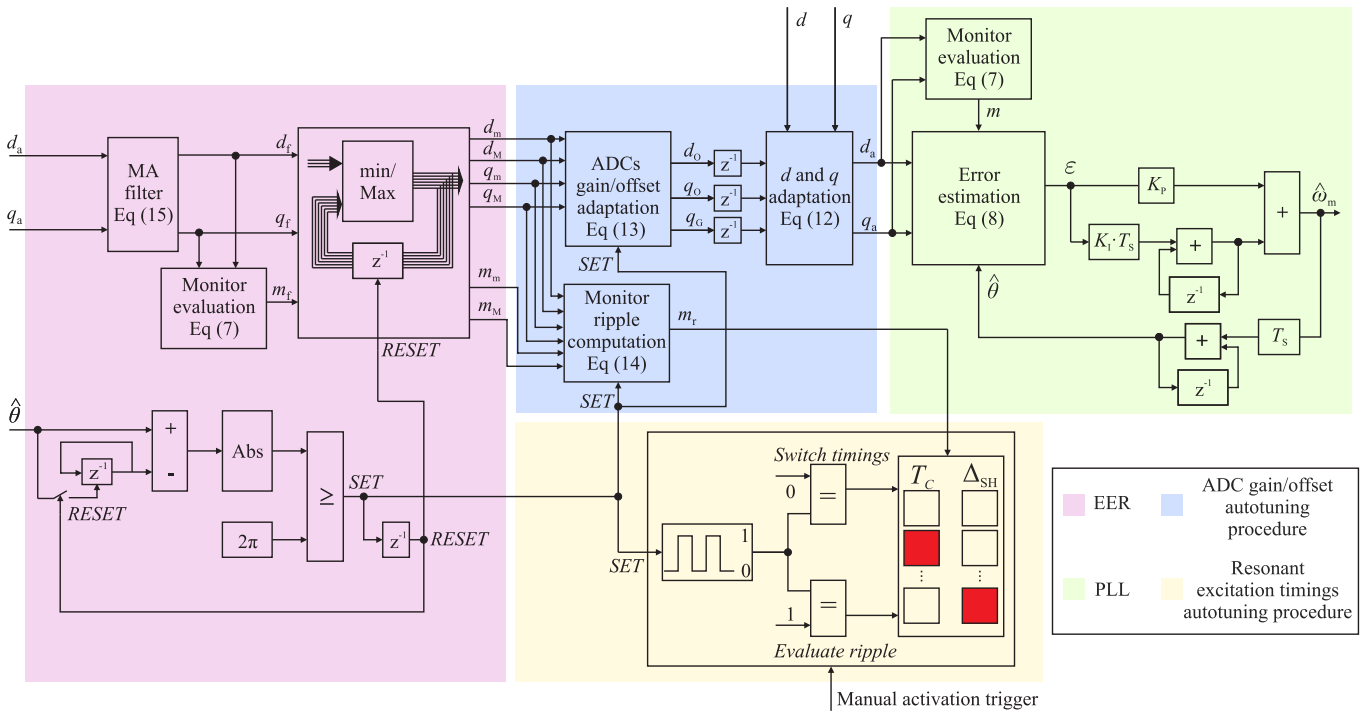

Fig. 7. Software processing block diagram.

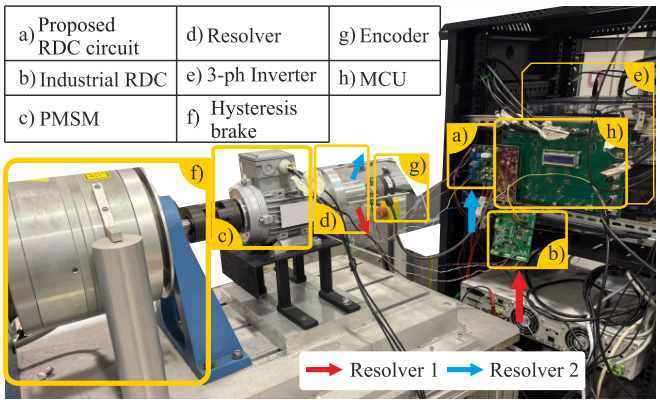

Fig. 8. Experimental setup.

architecture. The sampling frequency f_s has been set to 10 kHz.

By numerical investigation, effective values of excitation timings have been found to be around $T_C = 4\,\mu s$ and $\Delta_{SH} = 5.5\,\mu s$. This is confirmed by the experimental waveforms of Fig. 6. To highlight the effectiveness of the excitation timings autotuning procedure, the corresponding search ranges $[T_{C,m}, T_{C,M}]$, $[\Delta_{SH,m}, \Delta_{SH,M}]$ have been set loosely to [2, 6] and [1, 9] μs, with a resolution of 250-ns step, and a manual activation was triggered with the drive operating at a constant speed of 60 r/min. The procedure converged to $T_c = 4\ \mu s$ and $\Delta_{SH} = 4.5\ \mu s$. The little discrepancy in Δ_{SH} is justified on one side by the finite sampling window size of the differential ADCs (configured to 500 ns), on the other side by the measurement noise (see Section IV-F). Unless otherwise specified, the excitation timings of the embedded RDC have been kept at the latter values.

B. Angle Offsets Quantification

Let $\theta_{p,r}$, $\theta_{i,r}$, and $\theta_{r,r}$ be the raw angle positions supplied, respectively, by the proposed RDC, by the industrial RDC, and by the encoder (used as reference). Since each sensor zero position depends on the sensor's mechanical coupling process, a constant angle offset has to be properly added to the supplied position readings so that the resulting zero positions are aligned, i.e., the angle errors should be evaluated with respect to the processed positions

$$\theta_p = \theta_{p,r} + \theta_{p,o}, \theta_i = \theta_{i,r} + \theta_{i,o}, \theta_r = \theta_{r,r} + \theta_{r,o}. \qquad (17)$$

The required angle offsets have been quantified with the following procedure.

1) $\theta_{p,o}$ has been set so that when the motor is magnetized along the magnetic axis of phase 1, the resulting motor electric angle is 0.
2) $\theta_{i,o}$ and $\theta_{r,o}$ have been set so that at a constant speed of 60 r/min the errors $\theta_p - \theta_i$ and $\theta_p - \theta_r$, averaged over 100 mechanical revolutions, converged to 0.

Angular errors ε_p and ε_i of the proposed and industrial RDC are then evaluated as follows:

$$\varepsilon_p = \theta_p - \theta_r \qquad \varepsilon_i = \theta_i - \theta_r. \qquad (18)$$

C. Angular Error Dynamic Repeatability Test

The dynamic repeatability test evaluates the angular accuracy of the two resolver channels during continuous rotation at three different speeds (250, 500, and 1000 r/min) and two load conditions corresponding to 50% and 100% of the rated torque. For each combination of speed and torque presented in Table IV, a time window corresponding to 100 mechanical revolutions was acquired. For every individual revolution,

TABLE IV
DYNAMIC REPEATABILITY TEST OPERATING CONDITIONS

Test id number	Speed (rpm)	Torque (% of rated value)
1	250	50
2	250	100
3	500	50
4	500	100
5	1000	50
6	1000	100

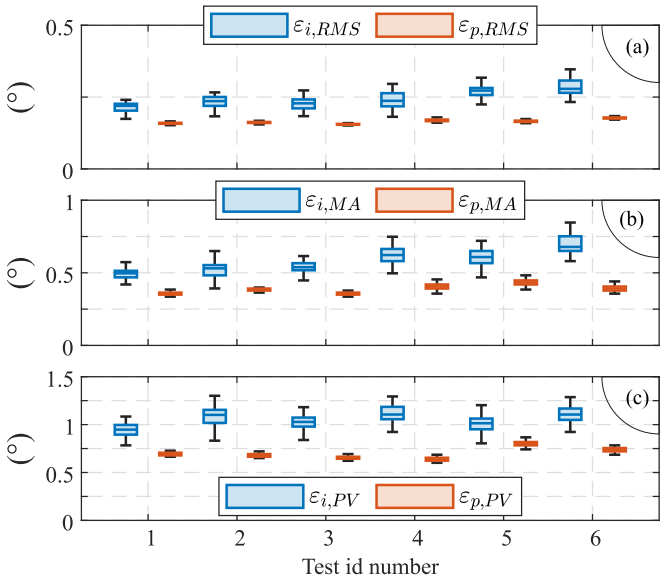

Fig. 9. Distribution of dynamic angular error over the operating conditions of the testbed. (a) Median and standard deviation of the RMS error, (b) maximum absolute error, and (c) peak-to-valley error.

three angular error metrics were computed: the rms angular error, the maximum absolute angular error, and the peak-to-valley angular error.

The median and standard deviation of each metric were then calculated for both RDCs from the distributions obtained from the acquired revolutions.

The results are shown in Fig. 9, which reports the median and standard deviation of the rms error [see Fig. 9(a)], the maximum absolute error [see Fig. 9(b)], and the peak-to-valley error [see Fig. 9(c)]. The comparison shows that the proposed RDC performs significantly better than the benchmark RDC with regard to all considered error metrics. Specifically, its performance depends only weakly on the operating conditions, while the benchmark RDC appears more sensitive to both load condition (a higher torque generates higher power-switching-induced noise) and speed condition (a higher speed generates higher motional-driven voltages in the resolver windings). Finally, the performance of the proposed RDC is more consistent across the overall testbed, as pointed out by the significantly smaller standard deviations.

Fig. 10 reports at 1000 r/min and 50% of the rated torque the time behavior over five resolver revolutions of the two resolver speed estimates [see Fig. 10(a)], of the angular errors [see Fig. 10(b)], of the conditioned sine/cosine voltages and the corresponding monitor signal [see Fig. 10(c)] and of the monitor signal zoomed in around its average value [see

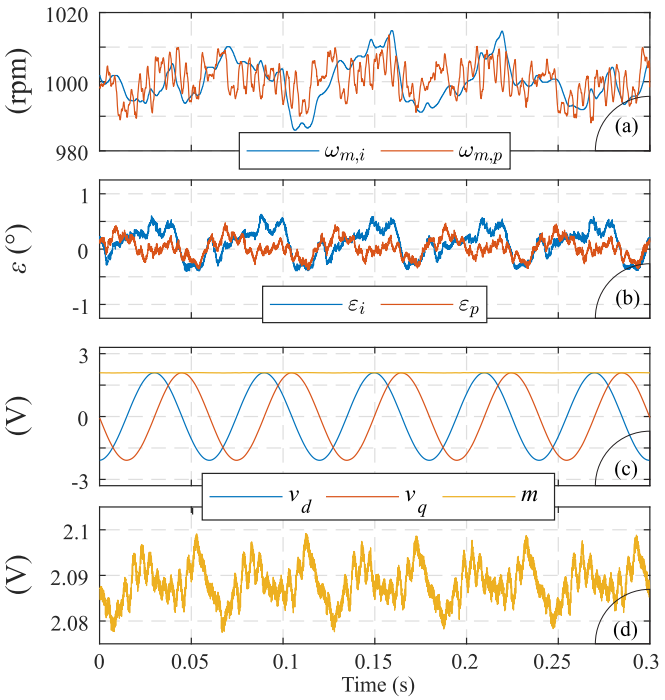

Fig. 10. Time behavior of angular errors and embedded RDC voltages at 1000 r/min and 50% of the rated torque over five mechanical revolutions. (a) Two resolver speed estimates, (b) angular errors, (c) conditioned sine/cosine voltages and the corresponding monitor signal, and (d) monitor signal zoomed in around its average value.

Fig. 10(d)]. Fig. 10(a) shows that the peak-to-peak ripples of the output speeds are comparable (about 1%). Conversely, from Fig. 10(b), it can be observed that the angle error delivered by the proposed RDC is kept under $\pm 0.4°$ while the one of the benchmark RDC goes beyond 0.5°. Given that the resolvers deployed on the experimental testbench are characterized by a maximum angular error of 0.3° while the encoder used as ground truth has an angular resolution of 0.09°, it can be concluded that the performance offered by the proposed RDC is, indeed, remarkable. Fig. 10(c) highlights the sinusoidal shape and the quadrature phase relation of the demodulated sine/cosine voltages, confirmed by Fig. 10(d), from which the ripple of the monitor signal can be estimated as less than 0.5%.

D. Angular Error Static Repeatability Test

This test evaluates the static positioning accuracy and repeatability under bidirectional motion. In this test, the FOC is configured in position mode and the position control variable is switched to the encoder channel. The motor was commanded to reach 18 angular positions spaced by 20°. Each position was reached ten times in the clockwise direction and ten times in the counterclockwise direction. For every positioning event, the angular error was recorded. The median and standard deviation were then computed from all measurements collected at each position. The procedure was performed for both resolver channels. Fig. 11(a) and (b) shows the distributions of the errors represented as box plots for the clockwise and the counterclockwise direction. The comparison confirms that the proposed embedded resolver solution achieves superior

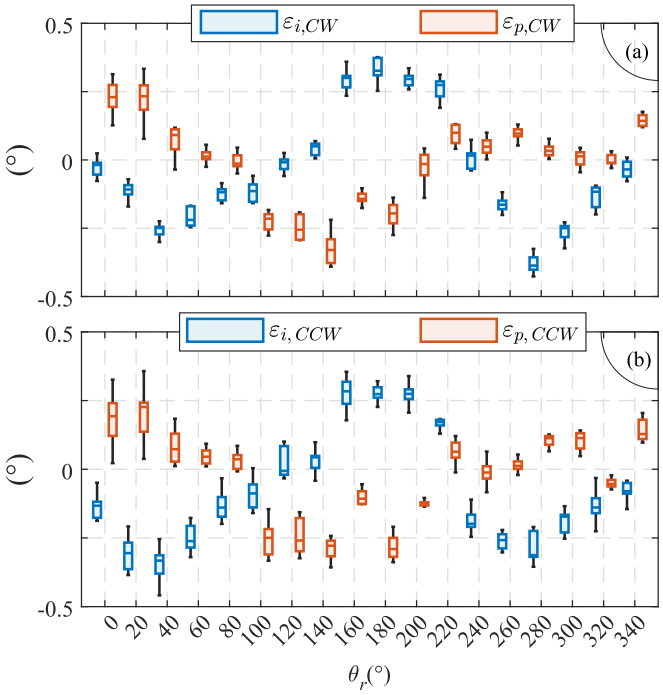

Fig. 11. Distribution of static angular errors over the target positions. (a) Clockwise direction and (b) counter-clockwise direction.

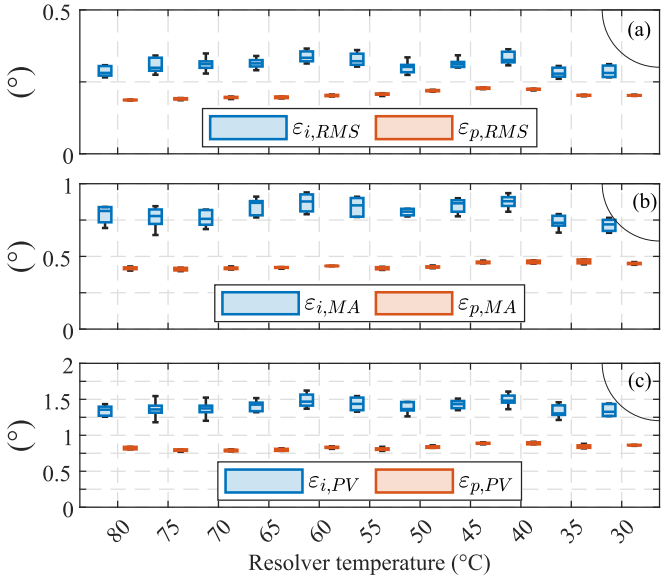

Fig. 12. Distribution of dynamic angular errors at 1000 r/min and 50% of the rated torque over the tested temperature range. (a) Median and standard deviation of the RMS error, (b) maximum absolute error, and (c) peak-to-valley error.

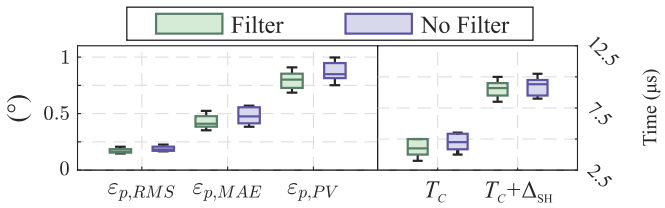

Fig. 13. Comparison of the distributions of dynamic angular errors and convergence excitation times at 1000 r/min with moving average filter enabled (green box) and disabled (blue box).

performance with respect to the median error behavior. Error dispersion and reciprocal motion consistency are comparable.

E. Thermal Sensitivity Test

The thermal test evaluates the sensitivity of the angular errors to variations of the resolver operating temperature. Starting from approximately 80 °C, as the temperature progressively decreased, angular errors of both RDCs were acquired with a 10 °C step over a time window covering 100 resolver revolutions at a constant speed of 1000 r/min. For each revolution, three angular error metrics were computed: the rms angular error, the maximum absolute angular error, and the peak-to-valley angular error. The median and standard deviation of each metric were then calculated for both RDCs from the distributions obtained from the acquired revolutions. The results are shown in Fig. 12, which reports the median and standard deviation of the rms error [see Fig. 12(a)], the maximum absolute error [see Fig. 12(b)], and the peak-to-valley error [see Fig. 12(c)]. As is evident, the angular error metrics remain substantially constant over the tested temperature range with very small deviation. This confirms the thermal robustness of the proposed resolver interface and demonstrates its insensitivity to temperature variations.

F. Measurement Noise Sensitivity Test

This test evaluates the sensitivity of the accuracy of the proposed excitation-timing autotuning procedure to measurement noise. With the motor operating at a constant speed of 1000 r/min, the autotuning routine was activated multiple times with the moving-average filter activated. Upon each routine convergence, three angular error metrics (rms, maximum absolute, and peak-to-valley) were computed over 100 mechanical revolutions. For each metric, the median and standard deviation were calculated. The same procedure was then repeated after disabling the moving-average filter, allowing a direct comparison between filtered and unfiltered conditions. Fig. 13 reports the angular error metrics together with the distributions of the convergence timings. The angular error results highlight marginal performance degradation without the filter, confirming the low sensitivity of the proposed resolver solution to measurement noise and further demonstrating the robustness of the approach, as confirmed by the corresponding timing distributions.

G. Acceleration Test

The acceleration test evaluates the tracking capability of the resolver during rapid speed transients. The speed, shown in Fig. 14(a), was increased from 0 to 1000 r/min by driving the rotor with the maximum torque (200%) and the brake mechanically decoupled in order to maximize the resulting acceleration. Fig. 14(b) shows the angular position errors for both resolver channels. The results show that the proposed RDC maintains a lower position error throughout the whole test. Indeed, while the angle error of the proposed RDC is kept low also in the initial acceleration phase, the angle error of the benchmark RDC is driven below −3° by the steep acceleration (about 50 000 r/min/s). The result is consistent

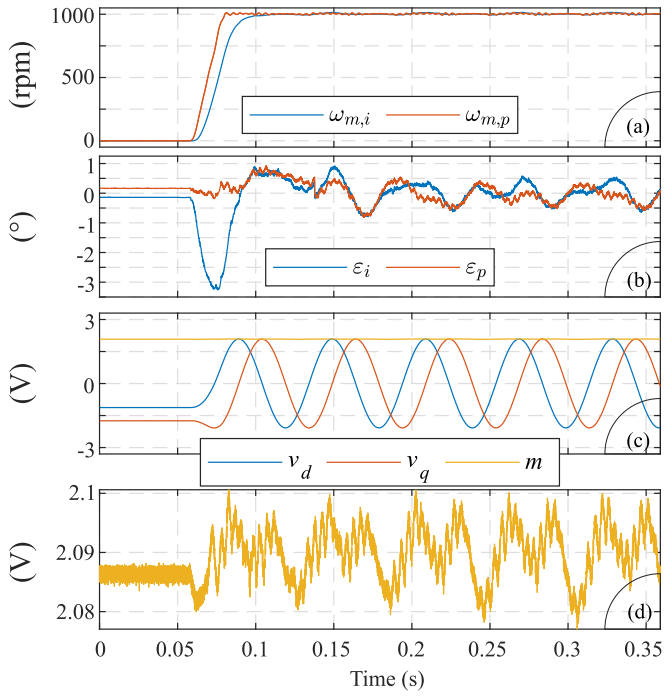

Fig. 14. Time behavior of speed, angular errors, and embedded RDC voltages during the acceleration test. (a) Speed, (b) angular position errors for both resolver channels, (c) monitor signals, and (d) monitor signals zoomed-in view.

with the speed behaviors of Fig. 14(a), which highlights a significant difference in speed tracking effectiveness. It should be pointed out that the software PLL bandwidth has been set to 250 Hz, while the tracking bandwidth declared for the benchmark IC in 16-bit mode is [100–350 Hz]. Demodulated sin/cosine voltages and the corresponding monitor signals are reported in Fig. 14(c) along with a zoomed-in view of the monitor signals in Fig. 14(d). It can be observed that the demodulation operates effectively even under heavy speed transients, as further confirmed by the ripple of the monitor signal, which can be evaluated, again, to be ≈0.5%.

V. Conclusion

We introduced an embedded RDC that replaces monolithic RDC ICs by combining resonant excitation, hardware-synchronized peak sampling, and quality-driven autotuning within the MCU. The experiments showed angular errors comparable with the tested resolver's accuracy, monitor signal ripple <0.5% and robust dynamics versus a commercial RDC-IC channel, at a lower cost and footprint. Unlike low-cost synchronous sampling [4], [18], our method engineers the excitation to place the maxima of sin/cos at S/H and optimizes timing via a measured-quality metric within a fully embedded MCU workflow. Unlike monolithic RDC ICs [3], it achieves comparable accuracy at reduced cost/area and with greater flexibility, at the price of careful excitation/analog co-design.

Appendix A
Influence of Phase 3 on the Maximum Excitation Current

At the start of phase 2 ($t = 0$), after the charge interval T_C, from the initial conditions $v_e(0) = v_C$ and $i_e(0) \approx v_C T_C / L_m$, the excitation current is driven by the resonant $L_m - C_R$ network with the following behavior (weak damping over the first quarter-cycle):

$$i_e(t) = I_e \sin(\omega_R t + \psi) \tag{19}$$

with $I_e = v_C \omega_R C_R (1 + (\omega_R T_C)^2)^{1/2}$ and $\psi = \arctan(\omega_R T_C)$.

In the absence of phase 3, the peak current $I_{e,pk}$ with amplitude I_e (or $I_e \exp[-\zeta(\pi/2 - \psi)]$ if a finite damping factor $\zeta \ll 1$ is considered) occurs at $t_{pk} = (\pi/2 - \psi)/\omega_R$.

If phase 3 is engaged at $t = T_R$, from $t \geq T_R$ the bridge forces a low output and C_R is actively discharged through R_C, arresting the oscillation. Thus, with regard to the effect on the maximum current within the cycle, two cases can occur.

1) *Case 1: $T_R \geq t_{pk}$ (Phase 3 After the First Peak):* In this case phase 3 does not reduce $I_{e,pk}$. It should be noted that, since phase 3 is engaged just after the SACs sampling, which should be triggered around the maximum of the differential amplifier outputs, this case never applies to properly configured excitation cycles.
2) *Case 2: $T_R < t_{pk}$ (Phase 3 Before the First Peak):* The peak current $I_{e,pk}$ is reached at the phase-transition instant $t = T_R$

$$I_{e,pk} = I_e \sin(\omega_R T_R + \psi). \tag{20}$$

Eventually, if a hard limit $i_e \leq I_{e,lim} \leq I_e$ must be observed while still sampling in phase 2, the maximum trigger time that guarantees the constraint (prepeak region) is

$$T_R^\star = \frac{1}{\omega_R}\left[\arcsin\left(\frac{I_{e,lim}}{I_e}\right) - \psi\right]. \tag{21}$$

If $T_R^\star \leq 0$, the limit is already violated at the start of phase 2. Practical remarks are given as follows.

1) The useful amplitude at the resolver outputs (and thus the monitor m) increases with I_e. However, as I_e increases, as per (21), $T_R^\star$ decreases, thus driving the SACs sampling instant away from the theoretical maximum of m. Therefore, C_R, v_C, and T_C should be sized so that $T_R^\star$ occurs just at the maximum of m while minimizing the duration of phases 1 and 2 (max SNR, shorter cycle).
2) An additional *active discharge* phase could be placed just after the *free evolution* substage of phase 4 to avoid the *residual resonance* substage, thus further shortening the excitation-cycle duration.

Appendix B
Maximum Achievable Excitation-Cycle Frequency

Three limits have to be taken into account.

1) *RMS/Thermal Limit:* If the resolver's losses in phase 1 are neglected, at the start of phase 2, the total energy stored in the system (magnetic component in the resolver and electric component in the resonant capacitor) can be expressed as follows:

$$E = \frac{1}{2} C_R v_C^2 \left(1 + (w_R T_C)^2\right). \tag{22}$$

In the worst case condition (phase 3 not used), E is wholly dissipated in the resolver over one excitation cycle. Therefore, the corresponding power losses are

$$P = Ef \tag{23}$$

with f the frequency of the cycle. Consequently, if P_N are the rated resolver's power losses, the following constraint applies:

$$f_{max}^{(rms)} \approx \frac{P_N}{E} \tag{24}$$

2) *Time/Kinematic Limit:* The period cannot be shorter than the sum of times for charge, rise to the resonant peak, discharge, and free evolution

$$f_{max}^{(time)} \approx \frac{1}{T_C + T_R + T_D + T_F}. \tag{25}$$

3) *Peak Current (No Saturation):* The phase 2 duration T_R, as per (21), must not exceed $T_R^\star$

$$T_R \le T_R^\star. \tag{26}$$

The maximum feasible excitation frequency is given by

$$f_{max} = \min\left\{ f_{max}^{(rms)},\ f_{max}^{(time)} \right\} \quad \text{with} \quad T_R \le T_R^\star. \tag{27}$$

Appendix C
Speed Influence on the Excitation Cycle

At nonzero speed, the voltages induced on the secondary windings of a resolver exhibit an additional motional term proportional to the speed itself, which adds to the transformer-related term. This introduces a position reading error whose magnitude depends on the method used to excite the resolver and to process the output signals.

In the case of a conventional RDC method based on an industrial chip, the voltages induced in the secondary windings take the following form:

$$\begin{cases} v_d \propto \omega \cos(\omega t)\cos\theta - \omega_m \sin(\omega t)\sin\theta \\ v_q \propto \omega \cos(\omega t)\sin\theta + \omega_m \sin(\omega t)\cos\theta \end{cases} \tag{28}$$

where the first term represents the transformer-related components, while the second term accounts for the motional components. From these relations, it can be observed that the weight of the motional terms with respect to the transformer-related ones is equal to ω_m/ω. Considering how the signals v_d and v_q are processed, it is possible to derive the estimation error as follows:

$$|\Delta\theta| \approx \frac{|\omega_m|}{\omega}. \tag{29}$$

By fixing the admissible angular error, for instance, $\omega_m/\omega < 0.01$ (i.e., angular error $\approx 0.5°$), it is possible to determine the maximum value of ω_m for which approximations (1) and (2) hold. In the case of an excitation frequency of 10 kHz, this corresponds to a maximum speed of 6000 RPM.

On the other hand, for the proposed method, the voltages induced on the secondary windings can be expressed as follows:

$$\begin{cases} v_d \propto \omega_R \cos\xi\cos\theta - \omega_m \sin\xi\sin\theta \\ v_q \propto \omega_R \cos\xi\sin\theta + \omega_m \sin\xi\cos\theta \end{cases} \tag{30}$$

with ω_R being the angular resonant frequency and $\xi = \omega_R t + \psi$. From these relations, it can be observed that the weight of the motional terms with respect to the transformer-related ones is equal to $\omega_m/\omega_R \tan\xi$. It is thus possible to obtain a lower weight either by setting $\omega_R > \omega$ and/or by considering that $\tan\xi < 1$ in the time window $[0, \Delta_{SH}]$, where Δ_{SH} is the acquisition instant. In view of the phase shift $\Delta\phi$ introduced by the filtering action performed on the signals v_d and v_q, it is possible to derive the estimation error as follows:

$$|\Delta\theta| \approx \frac{|\omega_m|}{\omega_R} \tan(\xi_{SH} - \Delta\phi) \tag{31}$$

where $\xi_{SH} \triangleq \omega_R \Delta_{SH} + \psi$. By comparison with the angular error associated with a conventional RDC method, it is evident that the proposed approach benefits from a double reduction. First, because it is possible to set $\omega_R > \omega$, and second, because the term $\tan(\xi_{SH} - \Delta\phi) < 1$ further contributes to reducing the error magnitude.

In the present work, $\omega/\omega_R \approx 0.7$ and $\tan(\xi_{SH} - \Delta\phi) \approx 0.69$. It follows that the angular error is slightly less than half of that obtained with the conventional approach. It also follows that the validity range is extended: for the same admissible angular error ($\Delta\theta < 0.01$ rad), the maximum speed is approximately 12 kr/min.

Appendix D
Temperature Influence on the Excitation Cycle

The resistance of the resolver windings varies with temperature according to the law

$$R(T) = R(T_0)\left[1 + \alpha(T - T_0)\right], \alpha \simeq 3.9 \times 10^{-3}\ °C^{-1}. \tag{32}$$

The resistance variation affects the real part of the input impedance [see (5)], thereby modifying the damping coefficient according to the following relationship:

$$\zeta = \frac{R_i}{2}\sqrt{\frac{C_R}{L_m}}. \tag{33}$$

Nevertheless, the resulting resonance angular frequency

$$\omega_R = \frac{1}{\sqrt{L_m C_R}}\sqrt{1 - \zeta^2} \tag{34}$$

remains weakly sensitive to temperature variations, since $\zeta \ll 1$.

In the present work, a temperature variation of 100 °C (i.e., $\Delta R = 40\%$) generates a resonance frequency variation of about 1%. This ensures a very small shift (less than 0.5 μs) of the peak of the sampled signals, maintaining a good signal-to-noise ratio without the need to repeat the autotuning procedure. This is confirmed by the experimental results presented in Section IV-E.

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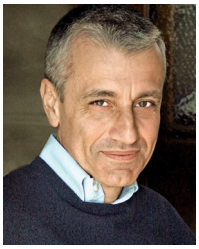

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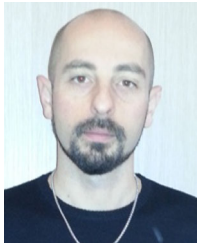

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