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Circuit-Based Electrothermal Simulation of Multicellular SiC Power MOSFETs Using FANTASTIC

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Abstract: This paper discusses the benefits of an advanced highly-efficient approach to static and dynamic electrothermal simulations of multicellular silicon carbide (SiC) power MOSFETs. The strategy is based on a fully circuital representation of the device, which is discretized into an assigned number of individual cells, high enough to analyze temperature and current nonuniformities over the active area. The cells are described with subcircuits implementing a simple transistor model that accounts for the utmost influence of the traps at the SiC/SiO₂ interface. The power-temperature feedback is emulated with an equivalent network corresponding to a compact thermal model automatically generated by the FANTASTIC tool from an accurate 3D mesh of the component under test. The resulting macrocircuit can be solved by any SPICE-like simulation program with low computational burden and rare occurrence of convergence issues.

Keywords: electrothermal (ET) simulation; finite-element method (FEM); model-order reduction (MOR); multicellular power MOSFET; silicon carbide (SiC)

1. Introduction

Silicon carbide (SiC) power devices are promising candidates for energy distribution, as well as for automotive, aircraft, and spacecraft applications, by virtue of their inherent features like high breakdown voltage, low on-state resistance, and excellent high-temperature capability [1].

Unfortunately, such devices often operate under critical conditions with a large amount of heat generation, which may lead to reliability degradation or even to an irreversible device failure in harsh cases. As a consequence, reliable simulation tools accounting for electrothermal (ET) effects are highly desired to define the thermal dissipation constraints and optimize the design of the transistor layout and/or of the cooling system. Such tools must be suited to describe temperature and current nonuniformities, which are often responsible for the safe operating area shrinking of transistors with a multicellular pattern. However, conceiving and developing a viable simulation strategy are challenging tasks due to multiple reasons. Fully numerical 3D ET analyses with device simulators concurrently solving the semiconductor and heat transfer equations are computationally unfeasible. Commonly-adopted approaches rely (i) on the interaction between a circuit simulation program and a 3D thermal-only numerical solver in a relaxation procedure [2,3], or (ii) on the extension of a finite-volume/-element software package to account for the electrical behavior of the transistor with simplified models [4,5]. However, for the specific case of SiC power devices, results can be

trustworthy only by using models that accurately describe the key physical parameters and their *non-intuitive* temperature dependences, which are rather different compared to the traditional silicon (Si) counterparts. In addition, regardless of the technology, the pre-processing geometry/mesh construction within the environment of the thermal solver is onerous and troublesome. Lastly, these approaches are very resource-hungry and prone to convergence failures, especially if dynamic simulations under critical conditions have to be performed.

In this paper, an innovative *circuit-based* ET simulation approach is proposed for multicellular SiC power MOSFETs, with the ambition of optimizing the trade-off between computational efficiency and accuracy. The strategy is articulated as follows: (i) the device is discretized into an assigned number N of individual cells (each associated to an independent heat source) described with a simple, yet accurate model accounting for the relevant influence of SiC/SiO₂ interface traps; (ii) the cell model is implemented with a SPICE-compatible subcircuit; (iii) an exceptionally accurate 3D finite-element method (FEM) description of the device is effortlessly obtained through a commercial solver aided by an *in-house* routine; (iv) the FANTASTIC code [6] is invoked, which *automatically* generates a dynamic compact thermal model (DCTM) of the device from the FEM representation, and thus builds an electrical network emulating the power-temperature feedback; (v) such a network is enriched with suitable voltage sources to account for nonlinear thermal effects, and the resulting circuit is referred to as *thermal feedback block*; (vi) a *purely-electrical macrocircuit* describing the whole ET behavior of the power device is constructed by connecting the N cell subcircuits to the thermal feedback block; (vii) the macrocircuit can be solved by *any* commercial circuit simulator in very short times and with unlikely occurrence of convergence problems. A multicellular 4H-SiC power MOSFET soldered on a direct bonded copper (DBC) substrate and operated under dc, short-circuit (SC), and unclamped inductive switching (UIS) conditions is considered as a case study.

This work extends the preliminary contribution [7], where a fully circuitual representation of the SiC power MOSFET was obtained and solved with a similar approach. However, the generation of the thermal feedback block, based on Foster networks, was carried out in a long pre-processing stage involving N 3D FEM transient simulations, as well as a procedure to determine the proper number of RC pairs of each network and identify their values; in addition, the thermal interactions among horizontally-far cells were either coarsely described or even disregarded.

The remainder of the paper is articulated as follows. In Section 2, the device selected to test the approach and the experimental setup are described. Section 3 offers details concerning the transistor model used for the elementary cells. Section 4 probes into the ET simulation approach. Results are reported and discussed in Section 5. Conclusions are then drawn in Section 6.

2. Device under Test and Experimental Setup

The whole analysis was performed on the CREE 4H-SiC vertical double-diffused MOSFET (VDMOS) denoted as CPMF-1200-S080B, rated 1200 V, 50 A, 80 mΩ, and targeted at solar inverters, high-voltage dc-dc converters, and motor drives. A top-view picture of the device under test (DUT) is given in Figure 1; indicated are the gate pad, the two source pads, and the gate interconnect tracks. The DUT presents a 4.08×4.08 mm² die area and a 3.46×3.46 mm² active area (there is a peripheral inactive region), the *effective* portion of which contributing to the current capability amounts to about 10 mm². The pattern is multicellular, with many thousands of body islands located in the N-drift region, within which there are source-body contacts surrounded by the polysilicon gate that lies beneath the source metal. The Ni/Ag drain contact is on the backside.

Isothermal measurements of I - V transfer and output characteristics of the bare die were performed by means of an *in-house* 250 A-rated curve tracer suited to apply down to 1 μs-wide current pulses, the device baseplate being set to assigned temperatures T_B through a thermochuck with 1 °C resolution. UIS experiments aimed at the evaluation of the breakdown voltage were carried out by a non-destructive custom tester [8]. The switching behavior was investigated by using a half-bridge converter board configured to perform a standard inductive load switching (ILS) test [9].

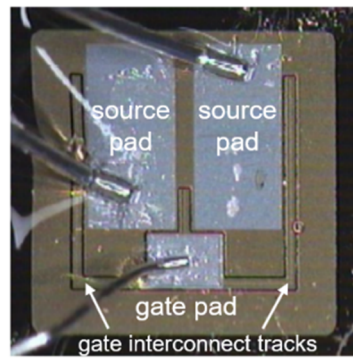


Figure 1. Device under test (bare die).

3. Transistor Model and Parameter Extraction Methodology

In the last decades, a noticeable effort has been made to develop models for SiC MOSFETs, a review of them being offered in [10]. Here we propose a slightly modified version of the behavioral model presented in [7,9] and used for ET simulations in [7,9,11]. Such a model, unlike those hitherto described in the literature, concurrently enjoys the following benefits: (i) it is simple, yet accurate enough, with a few parameters easy to extract; (ii) it can be implemented with a subcircuit compatible with *any* SPICE-like program; (iii) it includes all the key physical parameters and their specific temperature dependence up to very high temperatures; (iv) it also accounts for avalanche effects due to impact ionization (II); (v) the nonlinear nature of the intrinsic capacitances can be activated.

3.1. Transistor Model

The model is an enriched variant of the classic SPICE Level 1. In particular, the transistor is represented as the series of an “intrinsic” conventional MOSFET describing the channel behavior, and a resistance for the lowly-doped N-type epitaxial region, as depicted in Figure 2.

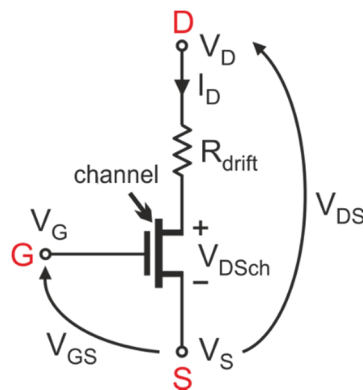


Figure 2. Sketch of the transistor representation.

Let us consider the following nomenclature:

- T [K] is the transistor temperature, assumed uniform in the regions impacting the device behavior.
- $T_0 = 300$ K is the reference temperature.
- $\Delta T = T - T_0$ [K] is the temperature rise over T_0 .
- T_B [K] the baseplate (and thermochuck) temperature.
- V_{GS} [V] is the gate-source voltage.
- V_{DS} [V] is the drain-source voltage.
- I_D [A] is the drain current.
- R_{drift} [Ω] is the bias- and temperature-dependent resistance of the N-type epitaxial drift region.

- $V_{DSch} = V_{DS} - V_{drift}$ [V] is the V_{DS} portion falling over the channel ($V_{drift} = R_{drift} \cdot I_D$).
- V_{TH} [V] is the temperature-dependent threshold voltage.
- K [A/V²] is the temperature-dependent current factor.

The channel region is described with the Level 1 model. If V_{DSch} is lower than the overdrive voltage $V_{GS} - V_{TH}$, the DUT operates in triode mode, and the II-free drain current I_{DnoII} is expressed as

$$I_{DnoII} = K \cdot \left[2 \cdot (V_{GS} - V_{TH}) \cdot V_{DSch} - V_{DSch}^2 \right] \quad (1)$$

Conversely, if $V_{DSch} \geq V_{GS} - V_{TH}$, then the DUT is driven into pinch-off, and

$$I_{DnoII} = K \cdot (V_{GS} - V_{TH})^2 \quad (2)$$

The negative temperature coefficient of V_{TH} is described through the following law:

$$V_{TH}(T) = [V_{TH}(T_0) - V_{TH\infty}] \cdot \exp(-a_{V_{TH}} \cdot \Delta T) + V_{TH\infty} \quad (3)$$

such an exponential model being an improvement with respect to the simple linear relationship used in [7].

The current factor K depends upon T since the electron mobility in the channel is temperature-sensitive; similar to [7,9], such a dependence is taken into account through the power relationship

$$K(T) = K(T_0) \cdot \left(\frac{T}{T_0} \right)^{-m(T)} \quad (4)$$

where the exponent $m(T)$ is

$$m(T) = -a_m + (a_m + b_m) \cdot \left[1 - c_m \cdot \exp\left(-d_m \cdot \frac{T}{T_0}\right) \right] \quad (5)$$

II effects are accounted for as follows [7,9]. The bias- and temperature-sensitive avalanche multiplication factor M (≥ 1) is given by [12]

$$M(V_{DS}, I_D, T) = 1 + m_{II} \cdot \tan \left\{ f_I(I_D) \cdot \frac{\pi}{2} \cdot \left[\frac{V_{DS} - R_{II} \cdot I_D}{BV_{DS}(T)} \right]^{m_{II}} \right\} \quad (6)$$

where $BV_{DS}(T)$ is the temperature-dependent drain-source breakdown voltage, expressed as

$$BV_{DS}(T) = BV_{DS}(T_0) \cdot \exp(\alpha_{II} \cdot \Delta T) \quad (7)$$

and $f_I(I_D)$ is a nondimensional correction term to describe a potential II dependence on current (i.e., on biasing conditions), given by

$$f_I(I_D) = \exp(\beta_{II} \cdot I_D) \quad (8)$$

Let us introduce the avalanche coefficient $\xi = M - 1$ (≥ 0). The II-affected drain current I_D is evaluated as

$$I_D = I_{DnoII} + I_{DII} = I_{DnoII} + \xi \cdot (I_{leak} + I_{DnoII}) \quad (9)$$

where I_{DII} is the additional current component only dictated by II, and I_{leak} is a small leakage current.

The resistance R_{drift} is expressed as the sum of (i) a bias- and temperature-dependent resistance R_{JFET} to model the path composed by the accumulation and JFET regions, and (ii) a temperature-dependent resistance R_{epi} for the epitaxial region beneath the JFET one [7,9]:

$$R_{drift}(V_{GS}, V_{drift}, T) = R_{JFET}(V_{GS}, V_{drift}, T) + R_{epi}(T) \quad (10)$$

where

$$R_{JFET}(V_{GS}, V_{drift}, T) = R_{JFET}(T_0) \cdot \left(\frac{T}{T_0}\right)^{m_{R_{JFET}}} \cdot \left(\frac{1}{1+V_1/V_{drift}}\right) \cdot \left(\frac{V_{GS}}{V_2}\right)^{-\eta} \quad (11)$$

$$R_{epi}(T) = R_{epi}(T_0) \cdot \left(\frac{T}{T_0}\right)^{m_{R_{epi}}}$$

$R_{JFET}(T_0)$ being the JFET resistance at $T = T_0$, $V_{drift} \gg V_1$, and $V_{GS} = V_2$ (V_1 and V_2 are fitting parameters). This formulation improves the one reported in [7] in the high-current triode region and is derived on the basis of simple arguments. First, the resistance of the accumulation region reduces with gate voltage due to the increased concentration of the attracted electrons; second, under high V_{drift} values, the high electric field occurring in the JFET region tends to saturate the electron velocity, thus degrading the mobility.

The dynamic transistor behavior is described by improving the Level 1 capacitance models; the nonlinear nature of C_{GD} and $C_{DS} = C_{DB}$ is accounted for with the following expressions [9]:

$$C_{GD}(V_{GD}) = (C_{GD0} - C_{GDMIN}) \cdot \left[1 + \frac{2}{\pi} \arctan\left(\frac{V_{GD}}{V^*}\right)\right] \quad (12)$$

and

$$C_{DS}(V_{DS}) = \frac{2}{\pi} \cdot C_{DS0} \cdot \left[\frac{\pi}{2} + \arctan\left(-\frac{V_{DS}}{V^{**}}\right)\right] + C_{DSMIN} \quad (13)$$

while C_{GS} was not modified [13].

3.2. Parameter Extraction Procedure

The threshold voltage V_{TH} and the current factor K were extracted in a very wide T_B range spanning from 300 to 500 K by resorting to the traditional *quadratic extrapolation method* [14,15] applied to I_D - V_{GS} transfer characteristics measured under isothermal (pulsed) conditions at $V_{DS} = 20$ V with the curve tracer mentioned in Section 2. Then the parameters in (3), (4), and (5) were calibrated so as to ensure the best matching between experimental data and the following relations:

$$V_{TH}(T_B) = [V_{TH}(T_0) - V_{TH\infty}] \cdot \exp[-a_{V_{TH}} \cdot (T_B - T_0)] + V_{TH\infty} \quad (14)$$

$$K(T_B) = K(T_0) \cdot \left(\frac{T_B}{T_0}\right)^{-m(T_B)} \quad (15)$$

with

$$m(T_B) = -a_m + (a_m + b_m) \cdot \left[1 - c_m \cdot \exp\left(-d_m \cdot \frac{T_B}{T_0}\right)\right] \quad (16)$$

The comparison between the measured V_{TH} and the optimized (14) is shown in Figure 3. It can be inferred that the DUT exhibits (i) a high $V_{TH}(T_0)$ (≈ 6.4 V) and (ii) a high negative temperature coefficient of $V_{TH}(T)$ at low/medium T_B compared to similarly-rated Si power MOSFETs. Both findings were attributed to the high density of SiC/SiO₂ interface traps (quantum states originating from the thermal oxidation of the SiC surface); more specifically, (i) electrons are captured by traps and do not contribute to channel formation, thereby leading to a high threshold voltage $V_{TH}(T_0)$, and (ii) V_{TH} markedly reduces with temperature due to the concurrent effect of more broken bonds that release electrons, and of the emission of inversion electrons from the traps, the latter effect being almost absent in the Si counterparts [16–18]. It must be underlined that the strong negative temperature coefficient in turn contributes to a significant positive temperature coefficient of I_D , which may exacerbate the ET feedback [19,20].

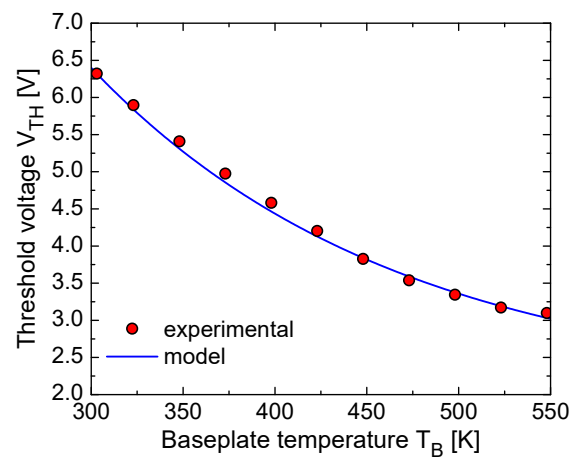


Figure 3. Threshold voltage V_{TH} vs. baseplate temperature T_B : comparison between experimental data (red circles) and model (14) (solid blue line) with optimized parameters.

The comparison between the measured K and model (15) and (16) with tuned parameters is shown in Figure 4. The temperature sensitivity of K is only related to that of the channel electron mobility μ_n , which is due to the interplay between (i) the Coulomb scattering with the filled (charged) interface traps, leading to a positive temperature coefficient induced by the trap discharging (release of electrons) with increasing temperature, and (ii) the acoustic-phonon scattering favoring a negative coefficient, where (i) prevails at low temperatures and (ii) dominates at high temperatures [18,21–23]. This behavior is accurately described by the m model (16).

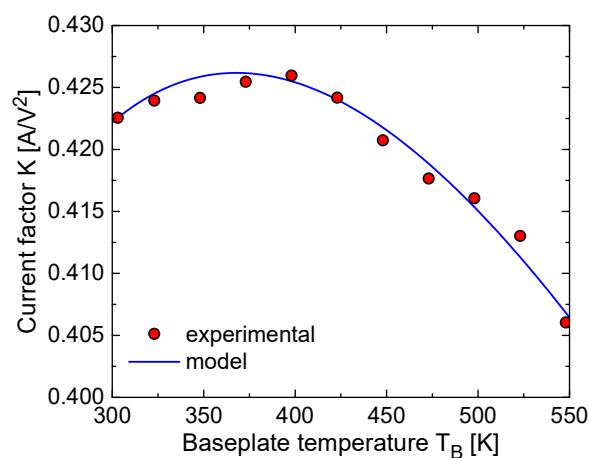


Figure 4. Current factor K against baseplate temperature T_B : comparison between experimental data (red circles) and model (15) and (16) (solid blue line) with optimized parameters.

The accuracy of the parameter calibration for the V_{TH} and K models is witnessed by the comparison reported in Figure 5 between (2) and the I_D – V_{GS} transfer characteristics measured under isothermal conditions at $V_{DS} = 20$ V and various T_B values in a current range wherein the DUT operates in pinch-off (note that $I_D \approx I_{DnoII}$). An inspection of the curves reveals the considerable positive temperature coefficient of I_D within a wide range of currents.

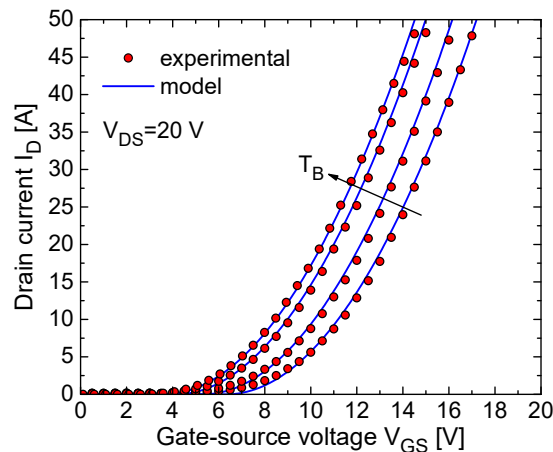


Figure 5. I_D - V_{GS} transfer characteristics of the DUT at $V_{DS} = 20$ V and $T_B = 303, 348, 423,$ and 473 K: comparison between experimental data (red circles) and model (2) with calibrated parameters for the V_{TH} and K formulations (solid blue lines).

The parameters of the drift resistance R_{drift} in (10), (11) were optimized by comparing the I_D - V_{DS} output characteristics at various V_{GS} and different T_B values in triode region with the model (1) applied to the scheme in Figure 2. Figure 6 reveals the accuracy of the extraction at $T_B = 303$ K.

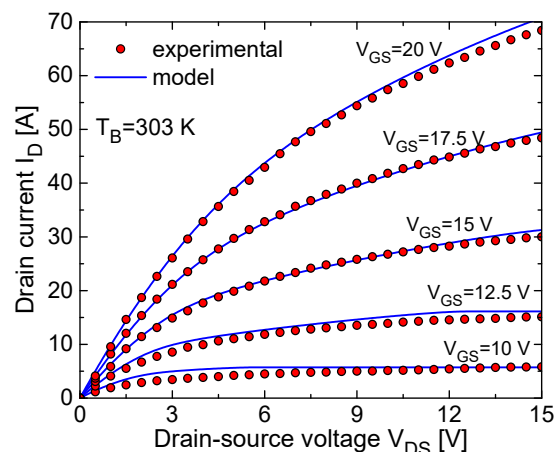


Figure 6. I_D - V_{DS} output characteristics of the DUT at $V_{GS} = 10, 12.5, 15, 17.5, 20$ V and $T_B = 303$ K: comparison between experimental data (red circles) and the model described in Section 2, where R_{drift} is given by (10), (11) with tuned parameters (solid blue lines).

The parameters of the II model given by (6) with (7) and (8) were tailored on the basis of experimental data determined under UIS conditions, and 2D numerical simulations of the T_B -dependent I_D - V_{DS} avalanche curve at $V_{GS} = 0$ V of an individual semi-cell of the DUT carried out with TCAD Sentaurus [24] (it must be remarked that the term “cell” here does *not* correspond to the discretization adopted in this work and identified by N , but it is one of the tens of thousands of identical blocks in which the effective active area of the MOSFET can be partitioned).

The parameters used in the expression of the capacitances C_{GD} (12) and C_{DS} (13) were calibrated to match the experimental gate and drain waveforms during an ILS turn-off and turn-on transient at different supply voltages.

All the optimized parameter values are reported in Table 1.

Table 1. Optimized parameter values used in the transistor model.

Parameter	Definition	Value
$V_{TH}(T_0)$	threshold voltage at reference temperature T_0	6.398 V
$V_{TH\infty}$	parameter of the threshold voltage model	2.05 V
a_{VTH}	temperature coefficient of the threshold voltage	6 mK ⁻¹
$K(T_0)$	current factor at reference temperature T_0	0.422 A/V ²
a_m	parameter of the exponent m accounting for the mobility temperature dependence	0.24
b_m	parameter of the exponent m accounting for the mobility temperature dependence	2
c_m	parameter of the exponent m accounting for the mobility temperature dependence	1.02
d_m	parameter of the exponent m accounting for the mobility temperature dependence	0.09
$R_{JFET}(T_0)$	resistance of the accumulation and JFET regions at reference temperature T_0 , $V_{drift} \gg V_1$, and $V_{GS} = V_2$	0.235 Ω
m_{RJFET}	exponent for the temperature dependence of the resistance R_{JFET}	-1.3
V_1	parameter to account for the R_{JFET} dependence on V_{drift}	13 V
V_2	parameter to account for the R_{JFET} dependence on V_{GS}	20 V
η	exponent to account for the R_{JFET} dependence on V_{GS}	3.45
$R_{epi}(T_0)$	resistance of the deep epilayer region at reference temperature T_0	10 m Ω
m_{Repi}	exponent to account for the potential temperature dependence of the resistance R_{epi}	0
$BV_{DS}(T_0)$	drain-source breakdown voltage at reference temperature T_0	1750 V
m_{II}	parameter of the avalanche multiplication factor M	1.8
n_{II}	parameter of the avalanche multiplication factor M	2.9
α_{II}	temperature coefficient of the breakdown voltage BV	0.18 mK ⁻¹
β_{II}	coefficient to account for the I_D dependence of factor M	0 A ⁻¹
R_{II}	resistance to account for the I_D dependence of factor M	10 Ω
C_{GDO}	zero-bias gate-drain capacitance	0.85 nF
C_{GDMIN}	minimum gate-drain reverse-biased capacitance	0.01 nF
V^*	gate-drain capacitance parameter	2 V
C_{DS0}	zero-bias drain-source capacitance	2.8 nF
C_{DSMIN}	minimum drain-source reverse-biased capacitance	0.06 nF
V^{**}	drain-source capacitance parameter	10 V

3.3. Impact of Interface Traps

The impact of the interface traps was investigated by resorting to the following strategy. The traps were virtually removed by (i) reducing $V_{TH}(T_0)$ to 4 V, (ii) decreasing a_{VTH} to 2 mK⁻¹, (iii) multiplying the current factor $K(T_0)$ by 50 to annihilate the degradation of mobility $\mu_n(T_0)$, and (iv) setting $c_m = 0$ to eliminate the influence of Coulomb scattering on μ_n , which will thus exhibit a negative temperature coefficient over the whole temperature range. Figure 7 shows the comparison between the *real* 4H-SiC DUT and the *ideal* traps-free counterpart in terms of transfer characteristics at $V_{DS} = 20$ V and various T_B values. It can be inferred that:

- differently from the DUT, which suffers from a marked positive temperature coefficient over the entire current range, the traps-free device is subject to a slight positive coefficient only at low drain current I_D (<20 A), where the negative temperature coefficient of V_{TH} prevails over the negative coefficient of μ_n , while beyond a zero-temperature coefficient region (also referred to as *compensation* region), the negative coefficient of μ_n dominates, and I_D reduces with temperature.
- the traps-free transistor benefits from a much higher current capability due to the lower V_{TH} and the higher μ_n .

To further corroborate the above findings, Figure 8 reports the temperature coefficient of the drain current I_D , given by [19,20,25]

$$\alpha_T = \left. \frac{\partial I_D}{\partial T} \right|_{V_{DS}} \quad (17)$$

for the real DUT and its traps-free variant at reference temperature T_0 and drain-source voltage $V_{DS} = 20$ V; it is again witnessed that the traps at the SiC/SiO₂ interface lead to a detrimental highly-positive α_T within a broad range of currents.

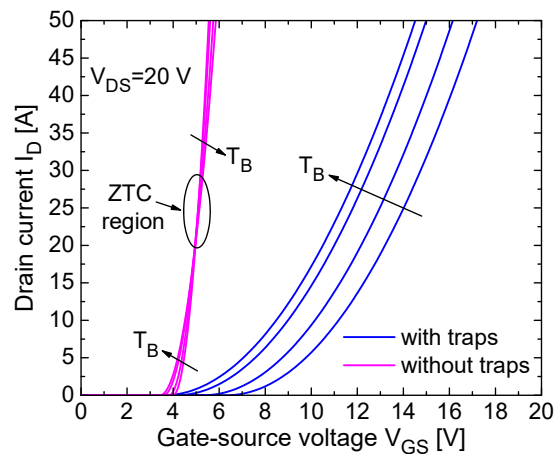


Figure 7. Modeled I_D - V_{GS} transfer characteristics at $V_{DS} = 20$ V and $T_B = 303, 348, 423,$ and 473 K: comparison between the real DUT (blue lines) and the traps-free counterpart (magenta). ZTC stands for zero-temperature coefficient.

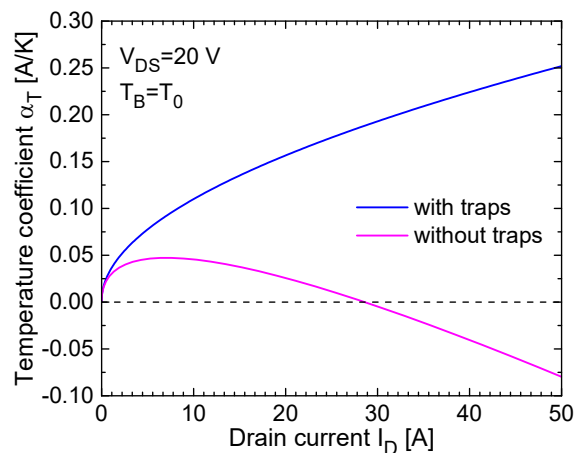


Figure 8. Temperature coefficient α_T of the drain current at $T_B = T_0$ and $V_{DS} = 20$ V for the real DUT (blue line) and its traps-free version (magenta).

4. Electrothermal Simulation Approach

We chose to resort to a *circuit-based* approach [7,11,26,27], which is a good trade-off between computational burden and accuracy. Such an approach makes use of the *thermal equivalent of the Ohm's law (TEOL)* and can be summarized as follows.

- The whole DUT is subdivided into an assigned number N of elementary cells, high enough to identify potentially-dangerous temperature gradients over the transistor active area, but not too high to prevent intolerably long CPU times or impossible memory storage. The individual cells are described with the model explained in Section 3, where the area-dependent parameters are properly scaled. For the simulation campaign reported in Section 5, all cells are assumed identical, although it is in principle possible to assign different parameter values to different cells to allow a statistical analysis of the influence of parameter fluctuations on the ET behavior of the component.
- Each cell is represented with a SPICE-compatible *subcircuit* implementing the above model through a *macromodeling technique*. The subcircuit makes use of (i) a standard MOSFET at reference temperature $T_0 = 300$ K as a “main” component to describe the channel region, and (ii) linear and nonlinear controlled sources to include all the model features that cannot be accounted for with the basic MOSFET, i.e., the temperature dependence of the threshold

voltage V_{TH} and of the current factor K , the bias- and temperature-dependent drift resistance R_{drift} , as well as the bias- and temperature-dependent II mechanism. The TEOL is adopted, namely, the temperature rise over ambient $\Delta T = T - T_0$ is actually a voltage, while the dissipated power P_D is treated as a current; this allows (i) enabling the temperature sensitivity of the key physical parameters, and (ii) describing the power-temperature feedback with an electrical network. Besides the standard electrical terminals (gate, drain, source/body), the cell subcircuit is also equipped with an input node carrying the “voltage” ΔT (provided by the thermal feedback block introduced below) and with an output node offering the “current” P_D (to be fed to the thermal feedback block).

- The power-temperature feedback (i.e., the dynamic heat propagation within the structure) is described with a TEOL-based SPICE-compatible thermal feedback block, which is composed by resistances, capacitances, and controlled sources. The inputs of this block are the powers P_D dissipated by the transistor cells (represented with currents), and the outcomes are the individual (nonlinear) temperature rises ΔT (emulated with voltages).
- The thermal feedback block contains an equivalent thermal network (i.e., a purely-electrical circuit relying on the TEOL). The main contribution of the proposed approach is that this network is *automatically* constructed in the pre-processing stage by invoking the FANTASTIC tool [6] (Section 4.3). FANTASTIC receives as an input an accurate 3D FEM representation of the domain, i.e., a mesh with information about (i) the discretization into elementary cells (each corresponding to an individual heat source), (ii) material parameters, and (iii) boundary conditions, and then extracts a reduced-order model and the associated network without the need of user’s expertise and COMSOL simulations; only 16 min were needed for the case study. The equivalent network accurately accounts for the self-heating of each cell and for the mutual interactions among *all* cells and describes the *linear* thermal problem. However, *nonlinear* thermal effects can be significant if the DUT is simulated under harsh conditions entailing high temperatures. In order to tackle this issue, a properly-tuned Kirchhoff’s transformation [28] is used, which converts the linear temperature rises (ΔT_{lin}) into their nonlinear counterparts (ΔT) through [29]

$$\Delta T = T_0 \cdot \left[m_k + (1 - m_k) \cdot \frac{\Delta T_{lin} + T_0}{T_0} \right]^{\frac{1}{1-m_k}} - T_0 \quad (18)$$

The calibration of the (positive) parameter m_k will be detailed in Section 4.2. Nonlinear voltage-controlled voltage sources emulating (18) are applied to the N temperature rise nodes of the equivalent thermal network; the resulting circuit is referred to as a thermal feedback block. It is worth noting that the FANTASTIC-based approach improves the strategy exploited in [7,26], where the thermal feedback block was based on Foster networks extracted in a rather long pre-processing stage from N onerous transient COMSOL simulations of the DUT (performed by activating one heat source at a time), and the thermal coupling between horizontally-far heat sources was roughly described or even neglected.

- The cell subcircuits are then connected to the thermal feedback block in a commercial circuit simulation tool (like PSPICE, LTSPICE, Eldo, ADS, SIMetrix); as a result, the whole domain under test, composed by the DUT soldered on a DBC substrate, is transformed into a *purely-electrical macrocircuit*, which suitably accounts for ET effects: the temperature, and thus the temperature-sensitive parameters, are allowed to vary during the simulation run. The solution of this macrocircuit under both static and dynamic conditions is demanded to the powerful and robust engine of the circuit simulation tool, with very low computational effort and minimized occurrence of convergence issues compared to other numerical methods.

The bias- and temperature-dependent R_{drift} described by (10) with (11) is taken into account by making use of source **D**, which imposes the voltage drop

$$V_{drift} = I_D \cdot R_{drift}(V_{GS}, V_{drift}, T). \quad (23)$$

Only half of the DUT was represented and simulated by exploiting its inherent symmetry. The effective active region ($\approx 5 \text{ mm}^2$) was partitioned into $N = 79$ cells, each with a $250 \times 250 \text{ }\mu\text{m}^2$ area (the procedure leading to the choice of the N value will be detailed in Section 4.4). As a consequence, compared to those reported in Table 1, the values of the area-dependent parameters were scaled by dividing the current factor and the capacitances by $2 \times N$, and multiplying the resistances by $2 \times N$. The popular commercially-available OrCAD PSPICE [30] was chosen to perform circuit simulations. The main schematic (resembling the actual layout) is represented in Figure 10, along with the corresponding cell numbering and a detail of the connections between adjacent cells. The drain current of the resulting macrocircuit (an outcome of the ET simulation) has to be multiplied by 2.

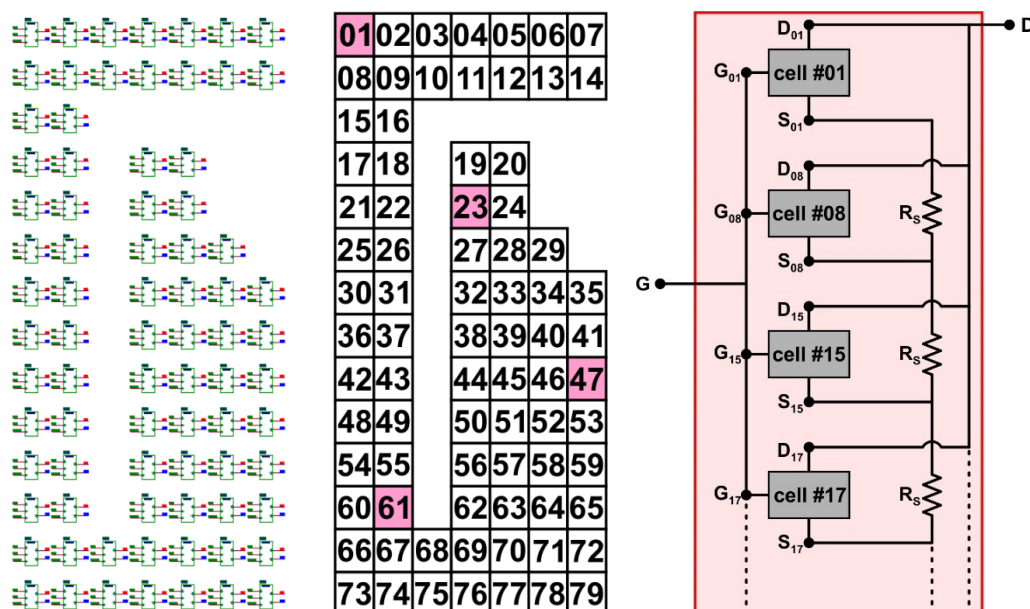


Figure 10. Discretization of the effective active area of half DUT. **Left:** PSPICE subcircuit with hierarchical blocks corresponding to the transistor cells; **center:** cell numbering, with evidenced cells of interest for the ET analysis presented in Section 5; **right:** connections between some adjacent cells.

4.2. FEM Representation of the Component under Test

Exhaustive details on the geometry and materials of the DUT (the CPMF-1200-S080B VDMOS) were taken from the datasheet and from reports available on a reverse-engineering website. The DUT was assumed to be soldered on a DBC substrate by means of a $50 \text{ }\mu\text{m}$ -thick tin-platinum alloy (SnPt) layer ensuring both mechanical joint and electrical connection with the drain [31]. Figures 11 and 12 show the top view and cross-section of the assembly, which enjoys the same symmetry of the DUT. The soldering process can be automated by means of thin SnPt films, which are preformed and match the size of the die; in addition, alignment masks are typically exploited to ease their positioning. The DBC is composed by two copper (Cu) sheets (namely, bottom and top plates) with a ceramic layer placed in between them. Such a layer provides dielectric insulation to the assembly and is realized with alumina (Al_2O_3) for the proposed case study; however, alternative materials like silicon nitride (Si_3N_4) [32] and aluminum nitride (AlN) [33] are also adopted in the DBC manufacturing process. The drain contact of the DUT is soldered on the top plate, while the bottom plate ensures a good thermal interface with the 3 mm-thick Cu baseplate.

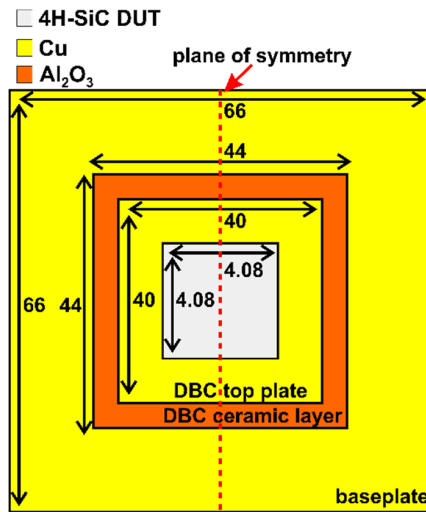


Figure 11. Sketch of the top view (not to scale) of the domain to be electrothermally simulated. All dimensions are expressed in mm.

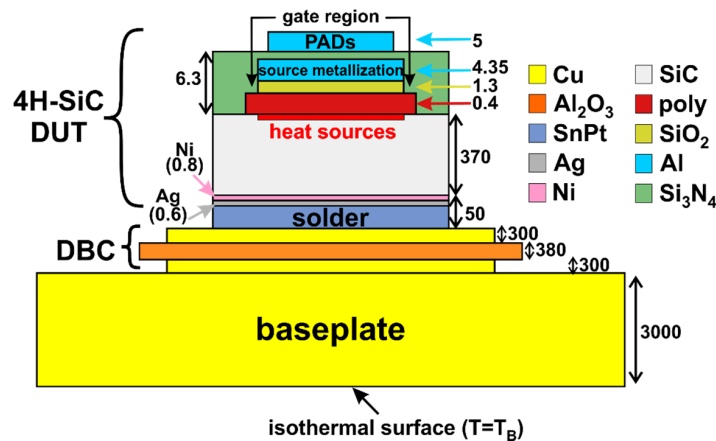


Figure 12. Sketch of the cross-section (not to scale) of the domain to be electrothermally simulated. All dimensions are expressed in μm .

The 3D domain was represented in the environment of the commercial FEM-based COMSOL Multiphysics software package [34] by means of the *in-house* routine detailed in [35], which allows *automatically* building an extremely accurate geometry (Figure 13) and performing a smart selective optimization of the tetrahedral mesh (Figure 14); this process conveniently avoids a painstakingly long and prone-to-errors manual procedure for geometry/mesh construction. The number of elements (tetrahedra) and degrees of freedom (DoFs) of the resulting grid are 3.8×10^5 and 5.2×10^5 , respectively. Figure 14 plainly illustrates that the mesh is highly fine over the die, while becoming gradually coarser by moving far away from the active region.

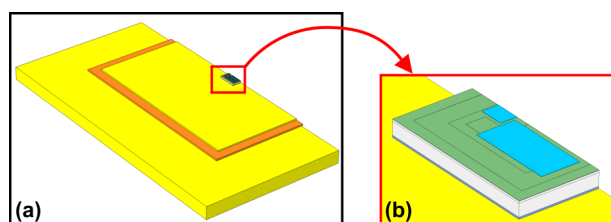


Figure 13. 3D representation of the geometry of the domain under test in the COMSOL Multiphysics environment (*draw mode*): (a) whole structure and (b) magnification of the 4H-SiC VDMOS die.

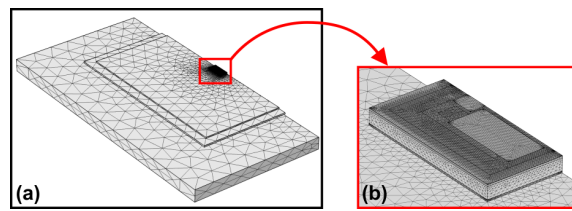


Figure 14. 3D tetrahedral mesh of the domain under test in the COMSOL Multiphysics environment (*mesh mode*): (a) whole structure and (b) magnification of the 4H-SiC VDMOS die.

As previously mentioned, all transistor cells (Figure 10) were individually associated to heat sources located over the top surface of the 4H-SiC DUT. In this representation, the heat is assumed to be dissipated over the whole effective active area, and not over the tens of thousands of individual channels; conveniently, this *unavoidable* approximation was demonstrated to be reasonable under dc and transient conditions (at least for not-too-short times) through a simulation analysis performed with TCAD Sentaurus and COMSOL. An isothermal boundary condition at $T_B = T_0$ was applied at the bottom of the assembly baseplate, whereas all other surfaces were assumed adiabatic (i.e., with zero outgoing heat flux). The material parameters adopted for the thermal simulations are listed in Table 2. Nonlinear thermal effects were accounted for by including the temperature dependences of the thermal conductivities described by

$$k(T) = k(T_0) \cdot \left(\frac{T}{T_0} \right)^{-\alpha} \quad (24)$$

$$k(T) = k(T_0) - \beta \cdot (T - T_0) \quad (25)$$

Table 2. Properties of the materials composing the assembly.

Material	$k(T_0)$ (W/mK)	c_p (J/KgK)	ρ (Kg/m ³)	α	β (W/mK ²)
4H-SiC	370 [36,37]	690 [37]	3211 [38,39] (value common to 4H-SiC and 6H-SiC)	1.29 [40]	
Al	240 [41]	905 [41]	2707 [41]		0.04 [41]
SnPt	68.8 [41]	228 [41]	7310 [41]		0.02 [41]
Ni	89.5 [41]	445 [41]	8906 [41]		0.08 [41]
Ag	427 [41]	236 [41]	10,524 [41]		0.07 [41]
poly-Si	40 [39]	920 [39]	2330 [39]		
SiO ₂	1.38 [39]	709 [39]	2203 [39]	-0.33 [39]	
Al ₂ O ₃	28 [39]	796 [39]	3900 [39]	1 [39]	
Cu	396.8 [41]	384 [41]	8954 [41]		0.05 [41]
Si ₃ N ₄	18.5 [39]	787 [39]	3100 [39]	-0.33 [39]	

It must be noted that (24) applies to semiconductors and insulators, while (25) is followed by some metals.

The pre-processing calibration of parameter m_k to be used for the Kirchhoff's transformation (18) was carried out with the following procedure. The domain under test was thermally simulated with COMSOL by varying the power P_D dissipated by the whole effective active area (described with only one heat source) over a wide range (0.1 to 573.5 W for half device, the latter value leading to a peak temperature of 1400 K); the thermal conductivity dependences upon temperature were either activated (*nonlinear* conditions) or deactivated (*linear* conditions). The average temperature rise over that area was determined for both cases. Then the Kirchhoff's transformation was applied to the linear temperature rise, and m_k was adjusted so as to obtain a good agreement between the nonlinear temperature rise computed by the transformation and the realistic one evaluated by COMSOL; it was obtained that

$m_k = 0.785$. The whole process lasted less than 1 h, as each nonlinear simulation was run in about 2 mins and 24 P_D values were applied.

4.3. FANTASTIC-Based Derivation of the Equivalent Thermal Network

The FANTASTIC tool, originally introduced by some of the authors in [6], where it was applied to merely-thermal 3D simulations of a state-of-the-art gallium-arsenide (GaAs) HBT, is based on the truncated balance (TRB)-based moment matching (MM) approach to model-order reduction (MOR) developed by one of the authors in [42].

In this tool, the dynamic heat conduction problem in a semiconductor device, assumed to be *linear*, is imported from either commercial (e.g., COMSOL) or open-source codes (e.g., SALOME SMESH), comprising: the mesh discretizing the geometry, as well as the definitions of heat sources, materials, and boundary conditions. Both hexahedral and tetrahedral meshes can be used. It is possible to define arbitrary heat capacity and tensorial thermal conductivity distributions. Neumann's, Dirichlet's, or Robin's boundary conditions can be applied. Superficial (i.e., indefinitely thin) and volumetric heat sources can be taken into account.

The FEM model of the thermal problem is then assembled by FANTASTIC. In particular, the mass matrix \mathbf{M} and the stiffness matrix \mathbf{K} are constructed. High-order basis functions can be used: most commonly, as a trade-off between efficiency and accuracy, tetrahedral meshes and second-order basis functions are considered. The M DoFs of the temperature rise distribution, forming the M -row vector $\vartheta(t)$, are solutions of the discretized linear dynamic heat conduction problem

$$\mathbf{M} \frac{d\vartheta}{dt}(t) + \mathbf{K}\vartheta(t) = \mathbf{q}(t) \quad (26)$$

in which the power density distribution vector $\mathbf{q}(t)$ takes the form

$$\mathbf{q}(t) = \mathbf{Q}\mathbf{P}(t) \quad (27)$$

where $\mathbf{P}(t)$ is an N -row vector with the powers dissipated by N independent heat sources, and \mathbf{Q} is an $M \times N$ matrix, the n -th column of which is the power density distribution vector of the n -th source, with $n = 1, \dots, N$. The port temperature rises of the N sources form the N -row column vector $\Delta\mathbf{T}(t)$ given by [42]

$$\Delta\mathbf{T} = \mathbf{Q}^T \vartheta(t) \quad (28)$$

As typical for MOR approaches, an $M \times \hat{M}$ matrix \mathbf{V} with $\hat{M} \ll M$ is defined, which allows approximating $\vartheta(t)$ by means of a reduced number \hat{M} of DoFs forming the \hat{M} -vector $\hat{\vartheta}(t)$, so that

$$\vartheta(t) = \mathbf{V}\hat{\vartheta}(t) \quad (29)$$

The \mathbf{V} matrix is used to project the heat conduction discretized problem (26)–(28) with the Galerkin's method, thus deriving a DCTM in the form

$$\hat{\mathbf{M}} \frac{d\hat{\vartheta}}{dt}(t) + \hat{\mathbf{K}}\hat{\vartheta}(t) = \hat{\mathbf{q}}(t) \quad (30)$$

being

$$\hat{\mathbf{q}}(t) = \hat{\mathbf{G}}\mathbf{P}(t) \quad (31)$$

$$\Delta\mathbf{T}(t) = \hat{\mathbf{G}}^T \hat{\vartheta}(t) \quad (32)$$

in which

$$\hat{\mathbf{M}} = \mathbf{V}^T \mathbf{M} \mathbf{V} \quad (33)$$

$$\hat{\mathbf{K}} = \mathbf{V}^T \mathbf{K} \mathbf{V} \quad (34)$$

are \hat{M} -order matrices, and

$$\hat{\mathbf{G}} = \mathbf{V}^T \mathbf{Q} \tag{35}$$

is an $\hat{M} \times N$ matrix. The \mathbf{V} matrix is determined by the algorithm reported below.

Algorithm 1: DCTM extraction

```

Set  $\mathbf{V} := \mathbf{0}$ 
for each independent heat source  $n=1, \dots, N$  do
1   Compute complex frequency values  $\sigma_p$  with  $p=1, \dots, P_n$ 
      for  $p=1, \dots, P_n$  do
          Set  $\hat{\Theta}_p = \mathbf{0}$ 
          if  $p > 1$  then
2             Solve compact model  $C_{p-1}$  given by (38) for  $\hat{\Theta}_p$ 
             Compute  $\tilde{\Theta}_p = \mathbf{V}_{p-1} \hat{\Theta}_p$  approximating  $\Theta_p$ 
3             Solve (37) for  $\Theta_p$  using  $\tilde{\Theta}_p$  as initial estimation in the iterative technique
4             Generate matrix  $\mathbf{V}_p$  spanning the columns of  $\mathbf{V}_{p-1}$  and  $\Theta_p$ 
5             Generate a compact model  $C_p$ , projecting (26)–(28) onto  $\mathbf{V}_p$ 
          Append the columns of  $\mathbf{V}_{P_n}$  to matrix  $\mathbf{V}$ 

```

At line 1 of the algorithm, the values σ_p , with $p = 1, \dots, P_n$, are automatically determined as a function of the desired relative error parameter ε as follows. First, the real positive quantities $\lambda_n < \Lambda_n$ are properly estimated for the heat conduction problem with respect to the power impulse thermal response of the current p -th heat source. Next, the value P_n is determined as the smallest integer such that

$$4 \exp(-P_n \pi^2 / \log(4/k')) \leq \varepsilon \tag{36}$$

being $k' = \lambda_n / \Lambda_n$. It is then set

$$\sigma_p = \Lambda_n \operatorname{dn} \left(\frac{2p-1}{2P_n} K, k \right)$$

with $p = 1, \dots, P_n$, in which K is the complete elliptic integral of the first kind of modulus k , and dn is the homonymous elliptic function of modulus $k = \sqrt{1 - k'^2}$.

At line 3, the temperature response to the n -th heat source is solved in the complex frequency domain at the frequency value σ_p . Thus, equation

$$(\sigma_p \mathbf{M} + \mathbf{K}) \Theta_p = \mathbf{Q} \mathbf{e}_n \tag{37}$$

is solved for Θ_p , \mathbf{e}_n being an N -row vector having all zero elements but one at the n -th row. Since the complex frequency values are real positive, the coefficient matrices of the resulting linear systems are symmetric positive definite, and the most efficient multigrid iterative solvers can be used for their solution.

At line 4, the \mathbf{V}_p matrix is achieved by appending to the columns of \mathbf{V}_{p-1} a vector derived orthogonalizing Θ_p with respect to the columns of \mathbf{V}_{p-1} .

At line 5, the DCTM C_p is determined proceeding as in (30)–(32), matrix \mathbf{V} in (33)–(35) being substituted by matrix \mathbf{V}_p .

At line 2, the temperature response Θ_p in the complex frequency domain due to the n -th independent heat source is estimated at σ_p using the DCTM C_{p-1} . To this aim, equation

$$(\sigma_p \hat{\mathbf{M}}_{p-1} + \hat{\mathbf{K}}_{p-1}) \hat{\Theta}_p = \hat{\mathbf{Q}}_{p-1} \mathbf{e}_n \tag{38}$$

is solved for $\hat{\Theta}_p$. This vector is used to determine the approximation $\tilde{\Theta}_p = V_{p-1}\hat{\Theta}_p$. At line 3 of the algorithm, such estimation of Θ_p is used to speed up the solution of (37) by setting the initial estimation of the solution.

It is noted that for the n -th heat source, with $n = 1, \dots, N$, the complex frequency values σ_p , with $p = 1, \dots, P_n$, are sorted in decreasing order. In this way, the linear systems introduced at line 3 of the algorithm are solved from the least to the most onerous ones in terms of CPU time. The computational burden is drastically reduced by this proper ordering, since the iterative solver can start from an estimate of the solution found in the previous step, which becomes increasingly accurate.

The DCTM achieved by this algorithm has dimension $\hat{M} = P_1 + P_2 + \dots + P_N$. Let $\mathbf{Z}(t)$ and $\hat{\mathbf{Z}}(t)$ be the N -th order power impulse thermal response [K/W] matrices of the discretized heat conduction problem (26)–(28) and of the DCTM, respectively. As shown in [43], it results in

$$\|\mathbf{Z}(t) - \hat{\mathbf{Z}}(t)\|_{\mathcal{H}_2} \leq 2\varepsilon\|\mathbf{Z}(t)\|_{\mathcal{H}_2}$$

being

$$\|\mathbf{Z}(t)\|_{\mathcal{H}_2} = \sqrt{\int_0^{+\infty} \text{tr}(\mathbf{Z}^T(t)\mathbf{Z}(t))dt}$$

the $\mathbf{Z}(t)$ Hankel norm. Similar results can be extended from the time to the frequency domain and can be stated for the whole spatial-temporal temperature distributions due to power impulses [43]. All these results provide a strong theoretical guarantee for the convergence of the method. As a consequence of (36), this convergence is very fast, being exponential with respect to the numbers P of σ_p , with $p = 1, \dots, P_n$. As a result, in practice accurate DCTMs can always be obtained with small space-state dimensions, \hat{M} .

It is now observed that by solving at limited cost the generalized eigenvalue problem

$$\hat{\mathbf{U}}^T \hat{\mathbf{M}} \hat{\mathbf{U}} = \mathbf{I}_{\hat{M}}$$

$$\hat{\mathbf{U}}^T \hat{\mathbf{K}} \hat{\mathbf{U}} = \hat{\mathbf{\Lambda}}$$

having as unknown the \hat{M} -order matrix $\hat{\mathbf{U}}$, in which $\hat{\mathbf{\Lambda}}$ is an \hat{M} -order diagonal matrix, and introducing the change of variables

$$\hat{\boldsymbol{\vartheta}}(t) = \hat{\mathbf{U}} \hat{\boldsymbol{\xi}}(t)$$

the DCTM equations (30)–(32) are transformed into

$$\frac{d\hat{\boldsymbol{\xi}}}{dt}(t) + \hat{\mathbf{\Lambda}} \hat{\boldsymbol{\xi}}(t) = \hat{\mathbf{\Gamma}} \mathbf{P}(t) \tag{39}$$

$$\Delta \mathbf{T}(t) = \hat{\mathbf{\Gamma}}^T \hat{\boldsymbol{\xi}}(t) \tag{40}$$

where $\hat{\mathbf{\Gamma}}$ is the $\hat{M} \times N$ matrix $\hat{\mathbf{V}}^T \hat{\mathbf{G}}$. The temperature rise distribution is then reconstructed as

$$\boldsymbol{\vartheta}(t) = \boldsymbol{\Xi} \hat{\boldsymbol{\xi}}(t) \tag{41}$$

$\boldsymbol{\Xi} = \mathbf{V} \hat{\mathbf{U}}$ being an $M \times \hat{M}$ matrix like \mathbf{V} .

Equations (39) and (40) can be interpreted as the equations ruling the equivalent network sketched in Figure 15.

Such a network, which can in principle describe the thermal behavior of *any* electronic component, is particularly suited to be solved by means of nodal analysis in SPICE-like simulators, since all elements are voltage-controlled current sources, and thus the number of variables is limited to \hat{M} . The topology is general and can be implemented into *any* circuit simulator.

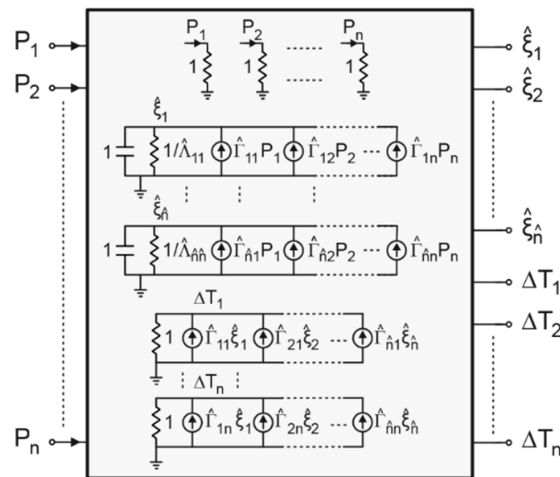


Figure 15. DCTM equivalent thermal network (after Codecasa et al. [6]).

4.4. Pre-Processing Evaluation of N and ϵ

During the pre-processing stage, two key parameters have to be chosen, namely, the number of elementary cells N ($=79$, as mentioned in Section 4.1) and the relative error parameter ϵ , the latter needed for the generation of the equivalent thermal network with FANTASTIC and set to 10^{-3} . For the particular component under test, this discretization and this error were found to be a good trade-off between accuracy and CPU time needed for the ET simulation, as evaluated in an additional pre-processing analysis where some N and ϵ values were tested; considering much higher N and/or much lower ϵ leads to a marginal accuracy improvement paid with a significant increase in CPU time.

4.5. Construction of the Macro-circuit

The macrocircuit representing the ET behavior of the packaged DUT was constructed in the PSPICE environment as follows. The linear equivalent thermal network, provided in the form of a netlist, was enriched with N nonlinear voltage-controlled voltage sources to account for the Kirchhoff’s transformation (18), and the thermal feedback block was thus obtained. It must be remarked that nonlinear thermal effects could in principle be accurately described by extracting a fully nonlinear equivalent thermal network with a variant of the FANTASTIC tool [11]. However, the complexity of the nonlinear network grows with the discretization N much more rapidly than that of the linear counterpart (used in this paper); for $N = 79$, such a network would be composed by about 32×10^6 elements, with insurmountable memory-storage problems. As a consequence, the adoption of a calibrated Kirchhoff’s transformation represents the only viable strategy to get accurate enough results. The ΔT and P_D nodes of the subcircuits (the individual transistor cells) were connected to the thermal feedback block. As shown in Figure 10c, all the gate terminals of the subcircuits were shorted together, as well as the drain and source ones, and it is possible to activate an electrical network to include the de-biasing over the source pad. A simplified scheme of the adopted strategy is shown in Figure 16.

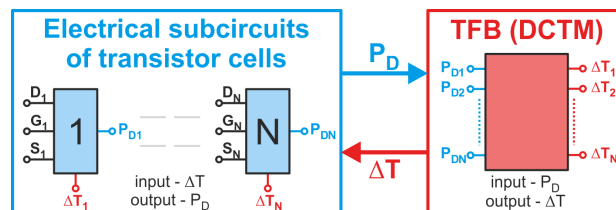


Figure 16. Schematic representation of the proposed strategy to perform a fully coupled ET analysis in a circuit simulation tool: the feedback loop between the electrical circuit (left) and the thermal feedback block (TFB, right) relying on the DCTM-based equivalent network is highlighted.

After the circuit simulation run, the whole spatial-temporal temperature rise distribution can be reconstructed in a post-processing stage at negligible computational cost and memory storage using (41).

5. Static and Dynamic Electrothermal Simulations

The whole pre-processing activity, involving isothermal measurements, optimization of the model parameters, geometry/mesh construction in COMSOL, proper domain discretization, equivalent network extraction with FANTASTIC, calibration of the Kirchhoff's transformation, and macrocircuit generation, can last a few days, after which *any* analysis can be performed in short times on the device of interest.

In particular, the macrocircuit was adopted to perform many PSPICE simulations of the DUT with DBC substrate in both static (dc) and dynamic conditions on a PC with an Intel Core i7-7700 (3.60 GHz) CPU and equipped with a 16 GB RAM. Unfortunately, experimental data for accuracy validation were not available for the examined component. On the other hand, the approach benefits from (i) a careful calibration of the transistor model from experimental data; (ii) a very accurate domain representation in COMSOL aided by the *in-house* routine mentioned in Section 4.2; (iii) an automated (and unaffected by user's errors) extraction of the linear equivalent network through FANTASTIC; (iv) a smart pre-processing calibration of the Kirchhoff's transformation. Hence, the only source of error can be induced by the degree of uncertainty concerning the thermal conductivities of the involved materials, which however affects any ET simulation approach.

First, the I_D - V_{DS} output characteristics were determined with a V_{DS} step amounting to 0.1 V under isothermal (at T_0) and ET conditions. Isothermal conditions were obtained by deactivating the thermal feedback block. The CPU time needed to simulate a single ET characteristic was nearly 100 s. Results are reported in Figure 17, which also shows the temperature rise above T_0 averaged over the effective active area (ΔT_{av}). It can be inferred that the simulation runs were stopped as ΔT_{av} reached 500 K.

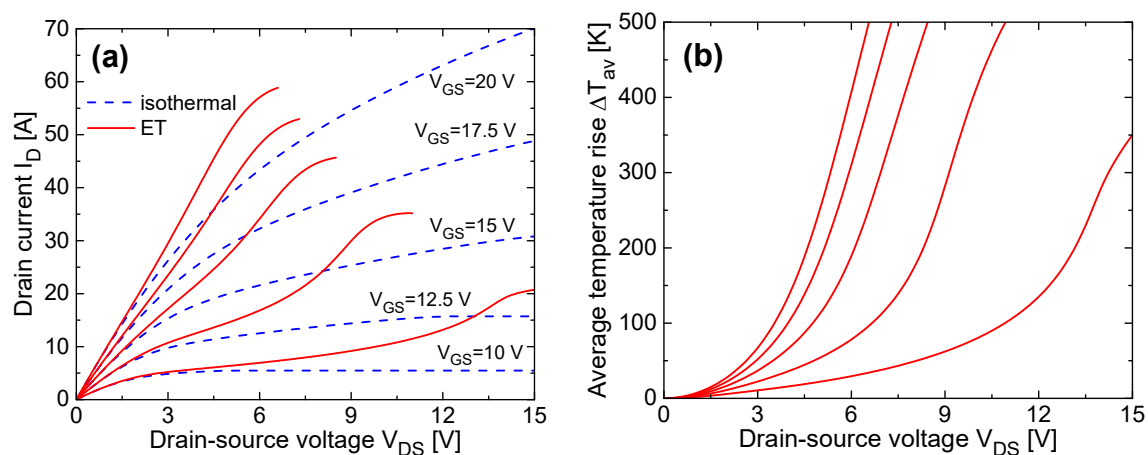


Figure 17. (a) I_D - V_{DS} output characteristics determined with the proposed approach under isothermal (dashed blue lines) and ET (solid red) conditions; (b) temperature rise $\Delta T_{av} = T_{av} - T_0$ corresponding to the ET conditions, T_{av} being the temperature averaged over the effective active area.

Afterward, SC tests were simulated. Such tests involve large power dissipation, and are typically used to quantify the device robustness under harsh and abnormal events (see e.g., [7,23,25,44–47], all focused on SiC MOSFETs). In the SC experiment, the DUT is first biased in the OFF state with a given supply voltage applied to the drain, and then turned on with a single gate pulse (a gate resistance R_{GATE} of 50 Ω was considered). The knowledge of the whole temperature distribution over the active area is important, since the value and position of the temperature peak are needed for reliability considerations. The effects of many combinations of gate and supply voltages were examined. Simulation runs were very fast: a single test required about 300 s with a fine time discretization.

The total drain current I_D conducted by the DUT vs. time is shown in Figure 18a for all the analyzed cases, while Figure 18b illustrates the corresponding temperature rises ΔT_{av} . The first figure reveals that I_D first grows due to the strong positive temperature coefficient induced by (i) the reduction in threshold voltage and (ii) the mobility increase (for the lowered Coulomb scattering), and then drops since the negative temperature coefficient triggered by the acoustic-phonon scattering dominates (thermally stable behavior) as all the traps have released electrons [7,25].

The temperature rises ΔT over cells #01, #23, #47, #61 (identified in the layout of Figure 10) are reported in Figure 18c for two cases, namely, $V_{GS} = 10 \text{ V}/V_{DD} = 200 \text{ V}$ and $V_{GS} = 20 \text{ V}/V_{DD} = 200 \text{ V}$. From the inspection of the waveforms, it is found that a pronounced temperature nonuniformity takes place in the first case (the inner cell #47 suffers from a ΔT two times higher than that of the top-corner cell #01), which can be explained as follows. The milder bias conditions ($V_{GS} = 10 \text{ V}$) allowed the device to safely undergo the test for a longer period, within which the heat had enough time to significantly spread, thereby favoring a stronger impact of the mutual thermal interactions and the consequent exacerbation of temperature gradients.

The whole temperature field in the domain was determined at chosen time instants from the DCTM generated with FANTASTIC in a post-processing step. More specifically, points A ($t = 25.5 \mu\text{s}$, $V_{GS} = 20 \text{ V}/V_{DD} = 200 \text{ V}$), B ($t = 338 \mu\text{s}$, $V_{GS} = 20 \text{ V}/V_{DD} = 50 \text{ V}$), and C ($t = 14 \text{ ms}$, $V_{GS} = 10 \text{ V}/V_{DD} = 50 \text{ V}$) identified in Figure 18a,b were selected, which approximately share the same ΔT_{av} value, i.e., 500 K. The computed temperature rise maps are shown in Figure 18d (top view) and Figure 18e (side view). As can be seen, despite the same ΔT_{av} ,

- point A, which falls at a time instant close to the beginning of the test, is endowed with a uniform and superficial temperature field, since the heat is still confined in the top active region close to the generation area;
- the temperature distributions in B and C are increasingly uneven, which is again ascribable to the much longer stress times. In particular, C suffers from a severe temperature focusing over the innermost DUT area, and—as witnessed by the side view—the downward heat had enough time to reach and hit the DBC.

Lastly, the macrocircuit was used to simulate two UIS tests, which are commonly adopted to evaluate the maximum amount of avalanche energy sustainable by the device [8,44]. In the UIS experiment, a load inductor L tied to the drain is first ramped up to a desired current by keeping the DUT in linear mode for a time t_{ON} ; then the DUT is turned off and brought into avalanche by the inductor, which preserves the current continuity. The tests will be hereinafter denoted as case #1 and #2, the specifics of which are as follows:

- case #1: $V_{DD} = 300 \text{ V}$, $L = 4.6 \text{ mH}$, $R_{GATE} = 15 \Omega$
- case #2: $V_{DD} = 600 \text{ V}$, $L = 12 \text{ mH}$, $R_{GATE} = 15 \Omega$

In both cases, a gate voltage equal to 20 V was applied for $t_{ON} = 200 \mu\text{s}$, and then lowered to 0. Again, the time elapsed by PSPICE for a single test was about 300–400 s. Concerning case #1, Figure 19a shows the drain current I_D and the drain-source voltage V_{DS} vs. time in the span 190 to 280 μs , while Figure 19b illustrates the temperature rises of cells #01, #23, #47, #61. An almost uniform temperature distribution was found, as witnessed by the map taken at time instant $t^* = 220 \mu\text{s}$, where the dynamic temperature averaged over the active area peaks (Figure 19c).

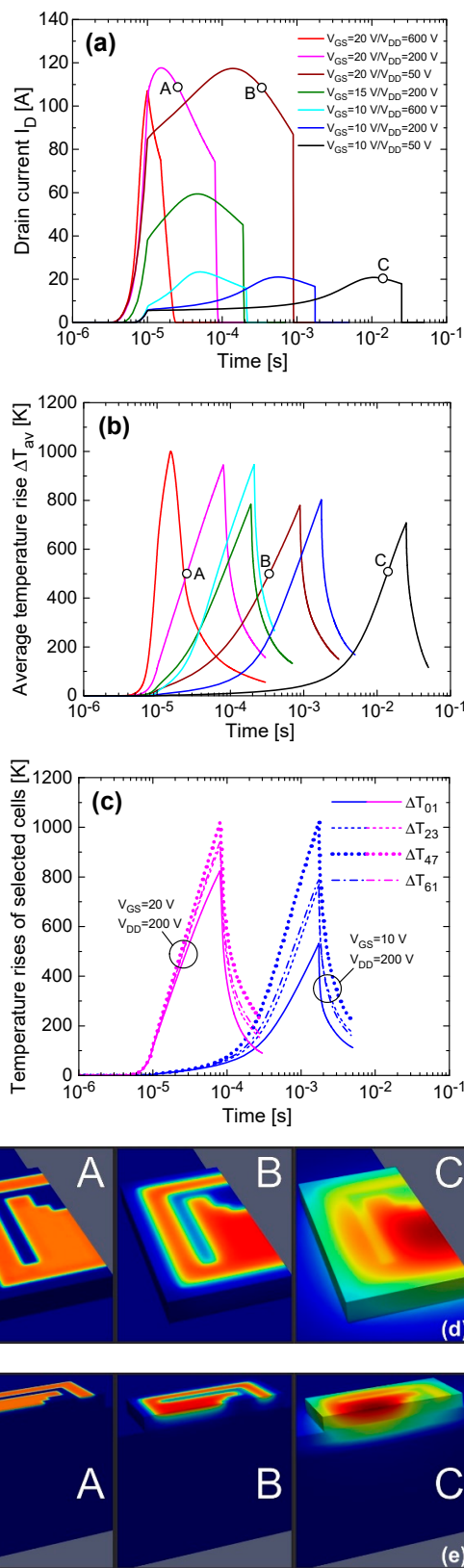


Figure 18. Simulated SC test: (a) drain current I_D vs. time for seven V_{GS}/V_{DD} combinations; (b) corresponding temperature rises averaged over the effective active area; (c) temperature rises of the individual cells highlighted in Figure 10 for 2 cases; (d) top and (e) side views of the 3D temperature rise maps determined at points A, B, and C shown in (a) and (b).

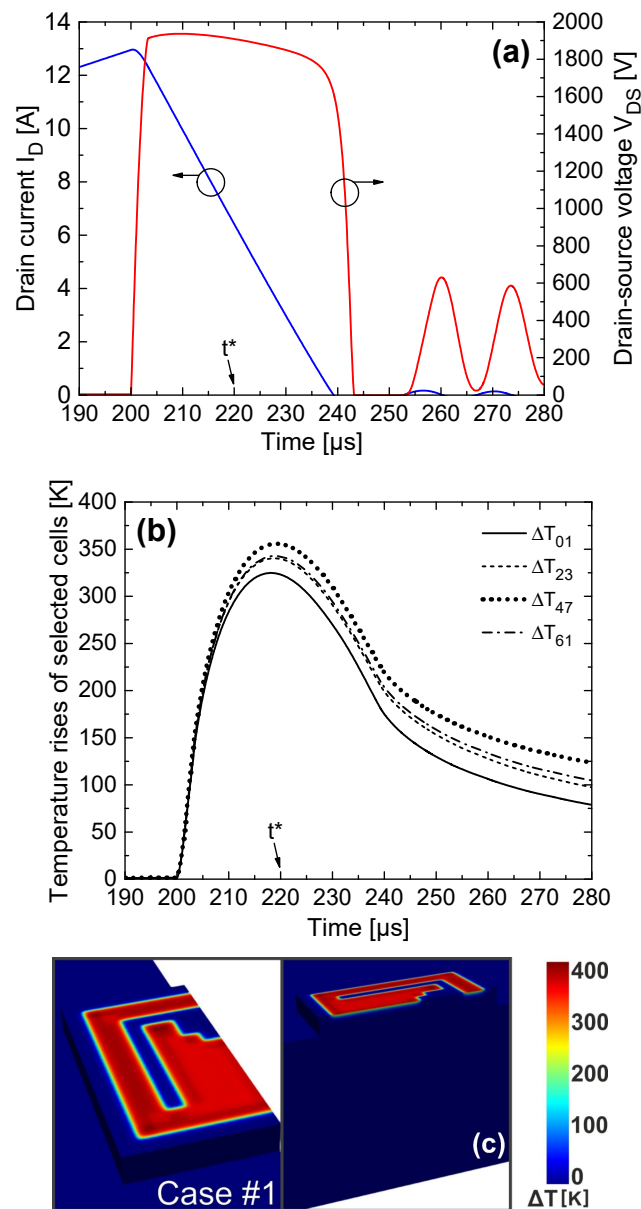


Figure 19. Simulated UIS test, case #1: (a) drain current I_D and drain-source voltage V_{DS} against time; (b) temperature rises of the individual cells identified in Figure 10; (c) top and side views of the temperature rise maps calculated at time instant $t^* = 220 \mu$ s shown in (a) and (b).

In case #2, despite the lower drain current $I_D \approx V_{DD} \cdot t_{ON} / L$ before turn-off (10 A instead of 13 A obtained for case #1), the average temperature reaches higher values due the longer discharging transient, in turn dictated by the higher L , since

$$\frac{dI_D}{dt} = -\frac{BV_{DS}(T) - V_{DD}}{L} \quad (42)$$

Results are shown in Figure 20. As can be inferred from Figure 20b, which reports the temperature rises of the selected cells, and from Figure 20c, which depicts the post-processing temperature maps at $t^* = 240 \mu$ s, a slightly more nonuniform temperature field occurs with respect to case #1.

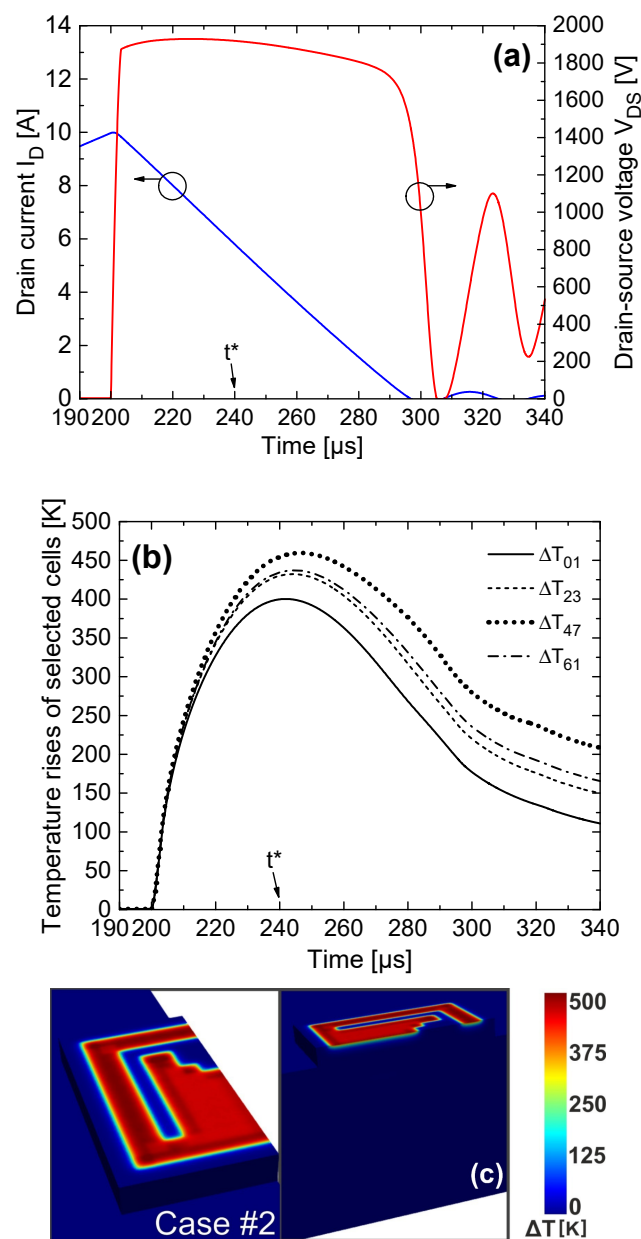


Figure 20. Simulated UIS test, case #2: (a) drain current I_D and drain-source voltage V_{DS} vs. time; (b) temperature rises of the individual cells highlighted in Figure 10; (c) top and side views of the temperature rise maps calculated at time instant $t^* = 240$ μs identified in (a) and (b).

6. Conclusions

In this paper, an advanced circuit-based approach for the static and dynamic electrothermal simulation of multicellular SiC power MOSFETs has been proposed, which—differently from the strategies encountered in the literature—seems to represent a good trade-off between accuracy and efficiency. The device is discretized into a chosen number of elementary cells (heat sources) and turned into a purely-electrical macrocircuit, where (i) the cells are described with subcircuits accounting for the key and harmful influence of SiC/SiO₂ interface traps, and (ii) the power-temperature feedback is modeled with an equivalent thermal network. This network is obtained through a *fully automated* process: first, a 3D mesh representing the device is generated in COMSOL with the support of an *in-house* routine that elaborates the layout files and makes use of further information about thickness of layers, position/shape of the heat sources, material parameters, and boundary conditions; then, such a mesh is provided as an input to the FANTASTIC tool, which derives a dynamic compact

thermal model of the device and the related equivalent network. The macrocircuit can be solved in the environment of *any* SPICE-like simulator with short CPU time and unlikely occurrence of convergence issues. The effectiveness and efficiency of the proposed strategy have been verified on a 1200 V, 50 A multicellular 4H-SiC VDMOS soldered on a DBC package. It has been shown that the simulation of short-circuit and unclamped inductive switching tests requires only 300–400 s on a normal PC, despite the critical conditions and the fine time discretization, and that potentially-dangerous temperature gradients/hogging can be easily identified. It can be concluded that the proposed approach can be helpful for industry engineers who are in charge of optimizing the thermal design of multicellular power devices in *any* technology.

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Nomenclature

AlN	aluminum nitride
Al ₂ O ₃	alumina
Cu	copper
GaAs	gallium arsenide
Si	silicon
SiC	silicon carbide
SiO ₂	silicon dioxide (or oxide)
Si ₃ N ₄	silicon nitride
SnPt	tin-platinum alloy
DBC	direct-bonded copper
DCTM	dynamic compact thermal model
DoF	degree of freedom
DUT	device under test
ET	electrothermal
FANTASTIC	FAst Novel Thermal Analysis Simulation Tool for Integrated Circuits
FEM	finite-element method
HBT	heterojunction bipolar transistor
II	impact ionization
ILS	inductive load switching
MM	moment matching
MOR	model-order reduction
MOSFET	metal oxide semiconductor field effect transistor
SC	short circuit
TEOL	thermal equivalent of the Ohm's law
TRB	truncated balance
UIS	unclamped inductive switching
VDMOS	vertical double-diffused MOS

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